2025 13th International Conference on Intelligent Embedded, MicroElectronics, Communication and Optical Networks (IEMECON) | 979-8-3315-7201-3/25/$31.00 ©2025 IEEE | DOI: 10.1109/IEMECON69302.2025.11365841

Design of Reversible Logic–Based Hybrid Adders for Low-Power VLSI and Quantum Applications

Shatavisha Dasgupta
Dept. of Electronics and Communication Engineering Institute of Engineering & Management, Kolkata School of University of Engineering an Management, Kolkata
Kolkata, India
dasguptashatavisha@gmail.com

Sourav Pandey
Dept. of Electronics and Communication Engineering Institute of Engineering & Management, Kolkata School of University of Engineering and Management, Kolkata
Kolkata, India
souravpandey9031@gmail.com

Debjit Roy
Dept. of Electronics and Communication Engineering Institute of Engineering & Management, Kolkata School of University of Engineering and Management, Kolkata
Kolkata, India
roydebjit2402@gmail.com

Agnik Maity
Dept. of Electronics and Communication Engineering Institute of Engineering & Management, Kolkata School of University of Engineering and Management, Kolkata
Kolkata, India
agnikmaity12@gmail.com

Antarik Sinha
Dept. of Electronics and Communication Engineering Institute of Engineering & Management, Kolkata School of University of Engineering and Management, Kolkata
Kolkata, India
antariksinha2017@gmail.com

Mihir Lal Saha
Dept. of Electronics and Communication Engineering Institute of Engineering & Management, Kolkata School of University of Engineering and Management, Kolkata
Kolkata, India
mihirlalsahaece@gmail.com

Abstract— **In modern Very-Large-Scale Integration (VLSI) systems, minimizing energy dissipation and information loss is a major challenge. Conventional logic gates suffer from irreversibility, leading to reduced efficiency in advanced computing applications. Reversible logic provides a promising solution by ensuring bijective input–output mapping, preserving information, and reducing heat generation. This paper presents the design of hybrid adder circuits—including ripple carry, carry skip, carry save, and carry select adders—using reversible logic gates such as Feynman, Fredkin, Peres, and HNG gates. The proposed designs focus on reducing quantum cost, garbage outputs, and ancillary inputs compared to conventional approaches. Simulation and synthesis were performed using Xilinx Vivado and ISE tools. Results demonstrate significant improvements, achieving a quantum cost as low as 28 for ripple carry and 45 for carry skip adder, while reducing the Total Reversible Logic Implementation Cost (TRLIC). These findings highlight the potential of reversible logic–based adders in low-power, high-performance VLSI and emerging quantum computing applications.**

Keywords— ***Reversible logic, Adder, Verilog, FPGA, Quantum Cost***

I. Introduction and Related Works

The two main issues with modern technology are energy dissipation and information loss. Reversible logic can be used to solve the issue [6]. A reversible logic gate has same number of inputs and outputs preventing loss of information and heat dissipation. Additionally, the output and input ports correspond exactly to one another. In order to facilitate the easy retrieval of inputs from outputs, the circuit operates backwards. A full adder is a crucial component in digital electronics which is used for the Arithmetic sum of the binary numbers. The origin of binary arithmetic has started since the 1800s. It was first described by the Gottfried Wilhelm Leibniz in the 17th century but it was actually implemented in the domain of computing in the 19th and early 20th century. The development of adders took place in the 1940s to 1950s whereas the advancement in semiconductor technology occurred in the year 1950 to 1980. After this development full adders became an important part of standard IC design and were extensively used in the microprocessor. A full-adder is a vital component in the domain of digital circuitry specifically in arithmetic logic units (ALUs). The following paper consists of improvisation of given three metrics. Low Quantum cost will lead to faster computation hence more accuracy with reduced error rates. It will also require lower resource requirements. Low Garbage output will lead to reduced complexity and will improve the efficiency of the circuit. It will also add better scalability to the circuit. Low ancilla input will lead to reduced qubit usage and lower resource cost along with the advantage of simplified error correction. The reduction of the quantum cost, garbage output and ancilla input will lead to improvement in the efficiency, scalability and reliability of the circuits. This will make the circuit perfect for practical applications where resources are limited and low error rates. This paper illustrates advanced designs of 4-bit adder which includes ripple carry adder, carry skip, carry select, carry save adders aiming to reduce certain parameters like Area, Power and Delay. The paper consists of improvised version of Carry Skip Adder using HNG, FEYNMAN, FREDKIN and PERES reversible logic gates. Carry Skip Adder is a binary adder which adds bits and allows the carry signal to skip a group of bits. This process can be carried out to reduce the delay. In the proposed design parameters like ancilla inputs, garbage output, quantum cost all three are reduced as compared to the existing work [2]. Carry Save Adder have a significant application in fields like cryptography, nanotechnology for its behaviour of optimizing parameters like speed and power. The

979-8-3315-7201-3/25/$31.00 ©2025 IEEE

fourth circuit is the design of 4-bit carry select adder using HNG and FREDKIN reversible logic gates. In the proposed design all the three parameters, ancilla input, garbage output and quantum cost are reduced and the TRLIC is also reduced to 98 [3]. The Total Reversible Logic Implementation Cost (TRLIC) is reduced to 65 which is less than that of existing work. The 4-bit ripple carry adder (RCA) is implemented using HNG and PERES reversible logic gates. The quantum cost of the proposed work is reduced as compared to the existing work. However, TRLIC for both the work is same [5]. Ripple Carry Adder plays a vital role in energy efficiency, and low power loss making it efficient for quantum circuit. The third circuit is the design of 4-bit carry save adder using PERES reversible logic gates. In the proposed design garbage output is reduced and the TRLIC is 64 [10]. Carry Select Adder have a significant application in low power VLSI by reducing dissipation of power and greater efficiency.

II. Fundamental Concept of Reversible Gates

In the field of VLSI technology, users encounter difficulties while using standard gates since they lose information after being used. As a result, Reversible logic gates can be considered now very helpful for the users because of their exceptional ability to function with reduced power consumption and no information loss. Therefore, reversible logic gates are regarded as extremely important components in the field of electronics. They also have a wide range of potential applications in cutting-edge fields such as low-power digital circuits and quantum computing. There's no fan out on reversible gates. Each reversible gate's input and output are mapped one to one, making them bijective in nature. High-performance chips release a lot of heat, which causes them to reach a limit beyond which we are unable to use it anymore. Because reversible circuits can retain information, they operate more easily and generate less heat. The ability of reversible logic gates to store data has allowed for the portability of numerous gadgets. Reversible logic gates are an extremely creative kind of logic gates in which each distinct collection of inputs results in a distinct set of outputs, and vice versa. As a result, these gates have the ability to recover inputs from outputs, which makes them invertible. It ensures that throughout calculation, no information is lost. By ensuring that no input set yields the same output and by saving input bits, they are able to make it a reality.

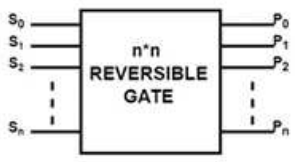

Fig.1 Basic Reversible logic

In the design of reversible logic gates, the three crucial matrices are:

(i) Quantum cost: The total number of Elementary Quantum Gates needed to implement a certain reversible logic gate is known as the quantum cost.

(ii) Garbage crucial outputs: These are undesirable results that reversible logic gates produce, but they are also to preserving the reversibility of these gates.

(iii) Ancilla input: This is the number of inputs that are kept constant at 0 or 1 in order to synthesize the specified logical function.

The effectiveness of reversible logic gates is determined by these three factors.

Several reversible logic gates which has been implemented in this work are as follows - .

A. Feynman Gate (FG)

The Feynman gate is a common type of reversible logic gate which consists of two inputs and two outputs terminals and is generally denoted by FG.

In the given below Fig.2, the terminals E and F represents the two input ports and the terminal M and N represents the two output ports.

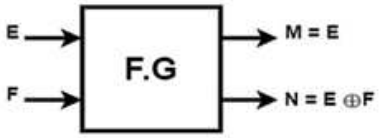

Fig.2 Feynman Gate

The output can be represented using the expression:

M=E, N=E□ F.

The quantum cost for Feynman gate is 1.

It can also act as an EX-OR gate for which N terminal will give us the desired EX-OR output.

TABLE 1. TRUTH TABLE OF FEYNMAN GATE

INPUT		OUTPUT	
E	**F**	**M**	**N**
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

B. Peres Gate

The Peres gate, which is typically represented as PG, is a highly helpful reversible logic gate with three input and three output terminals.

The three input ports are represented by terminals E, F, and G in the supplied Fig. 3.

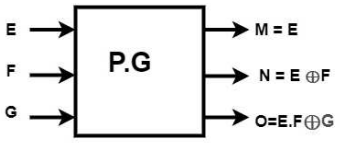

Fig.3 Peres Gate

While the three output ports are represented by terminals M, N and O. The following expression can be used to describe the output:

M=E, N=E⊕F, and O=E.F⊕ G

For the Peres Gate, the quantum cost is 4.

It may be used as an AND gate in addition to being heavily utilized in the construction of adder circuits.

The outputs of the Peres gate will change to M=E, N=E⊕F, and O=E.F when I=0 is applied. The desired AND gate output will be provided via the L terminal.

TABLE 2. TRUTH TABLE OF PERES GATE

INPUT			OUTPUT		
E	**F**	**G**	**M**	**N**	**O**
0	0	0	0	0	1
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1

C. Hng Gate

The HNG Gate is a type of reversible logic gate which consists of four inputs and four outputs terminals.

In the given below Fig. 5., the terminals G, H, I&J represents the four input ports and the terminal K, L, M & N represents the four output ports.

The output can be represented using the expression:

K=G, L=H□ H, M = G □ H □ I and N= (G □ H).I □ G.H □ J

The quantum cost for HNG Gate is 6.

It can also be used for the designing of adder circuits. Putting J=0, the HNG Gate outputs will be altered and M terminal will give us the desired SUM output whereas the N terminal will give us the desired CARRY output.

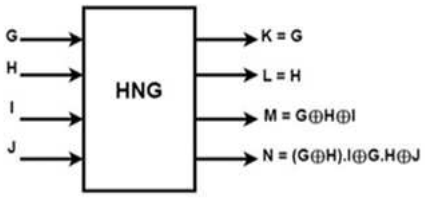

Fig.4 Hng Gate

TABLE 3. TRURTH TABLE OF HNG GATE

INPUT				OUTPUT			
G	**H**	**I**	**J**	**K**	**L**	**M**	**N**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1

D. Fredkin Gate

The Fredkin Gate, commonly represented by FDG, is a kind of reversible logic gate with three input and three output terminals.

The three input ports are represented by terminals G, H, and I in Fig. 4., while the three output ports are represented by terminals J, K, and L.

The output can be represented using the expression:

J=G, K=G′.H □ G.I, and L=G′I □ G.H

For Fredkin Gate, the quantum cost is 5.

It is mostly utilized in the construction of multiplexers, where Terminal G serves as the select line and Terminals H and I serve as the two mux inputs.Depending on the value of G, the output port will be chosen.

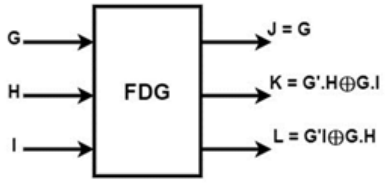

Fig.5 Fredkin Gate

TABLE 4. TRUTH TABLE OF FREDKIN GATE

INPUT			OUTPUT		
G	**H**	**I**	**J**	**K**	**L**
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1

III. DESIGN METHODOLOGY

A basic digital circuit used in digital electronics and computers to add binary integers is called a complete adder. It requires three inputs: a carry input (C_{in}) from a previous stage and two four-bit values named A_1, A_2, A_3, A_4 and B_1, B_2, B_3, B_4 respectively. Two outputs are produced by the full adder: a carry-out bit (C_{out}) that signals if there is a carry-over to the next more important bit position, and a sum bit (S) named as S_1, S_2, S_3, S_4 respectively, which is the least significant bit of the addition result. A truth table that determines the output depending on the mix of inputs defines how a complete adder operates. It makes use of simple logic gates like AND for carry computation, XOR for sum calculation, and OR for combining carry outputs.

In particular, AND gates are used to determine the carry-out bit (C_{out}), which produces a carry when two or more inputs are high, whereas XOR gates are used to compute the sum bit (S). This circuit is essential to processors and microcontrollers' arithmetic logic units (ALUs), enabling binary addition operations that are necessary for digital

computation in a variety of applications, such as computers, calculators, and other digital devices.

In comparison to a single-bit full adder, a 4-bit full adder is a more complex digital circuit that can add four sets of binary digits (each set made up of a bit from A, B, and a carry-in), as well as produce four sums and a final carry-out. The following is a thorough explanation of a 4-bit full adder:

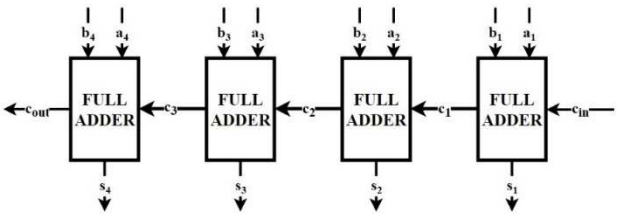

Fig. 6. Block Diagram of 4-bit Full Adder

IV. Proposed Hybrid Adder Architectures

A. Carry Skip Adder

A carry skip logic is a special type of logic circuit where it determines if a block of bits can be skipped during the carry. The first step is to generate and propagate; the generated signal indicates if a carry will be generated for each bit and the propagated signal indicates if a carry will be passed via that bit position. Skip logic determines whether the carry can be skipped by examining a block's propagated signal [2]. The carries are skipped to the following block if every propagated signal in a block is high, it will pass the carry. Carry skip adder is a form of binary added circuit. In this paper, a 4-bit CSA (Carry Skip Adder) is designed using a combination of 4 HNG gate,4 Feynman gate, 3 Peres gate and 1 Fredkin gate. Carry skip adder provides better performance than ripple carry adder as it reduces delay [1]. A carry bit in ripple carry adder is delayed until the carry bit from the preceding bit addition is available which may lead to propagation delay. This latency is decreased using a carry skip adder. A carry skip adder can skip over bit groups when it has its ability. Carry skip adder is a combination of ripple carry adder along with carry skip logic. In this carry skip adder, in HNG_1, A_0 and B_0 are taken as inputs where the third input is 'C_{in}' and fourth input is taken as '0' whereas R_0 (SUM) is output and S_0 is carry which is again taken as input for the next HNG_2 gate block. P_0 and Q_0 of the HNG_1 is carried next onto the Feynman gate. In this design Feynman gate acts as a XOR gate. Similarly in this way all the operations are carried out in each pair of HNG and Feynman gate to provide the desired inputs of the Peres gate. Here Peres gate acts as an AND gate. The outputs are then passed on to the FDG (Fredkin gate) where it produces output as 'C_{out}'. FDG acts as a multiplexer. In this circuit the total number of garbage outputs are '12', ancilla input is '7' and the quantum cost is reduced to '45'.

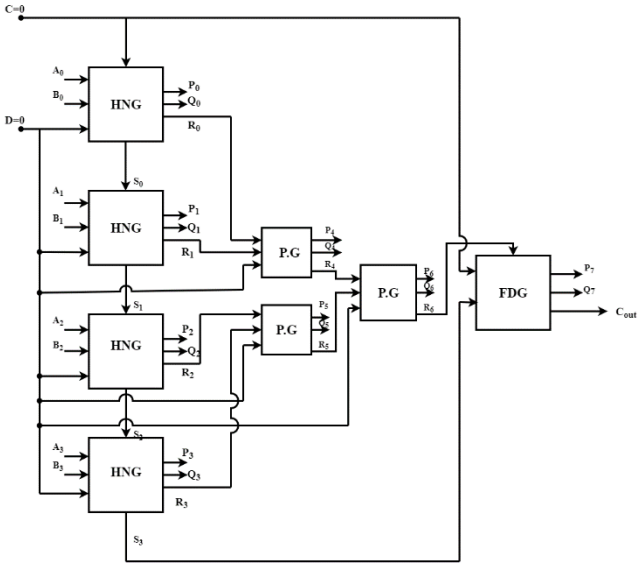

Fig.7 Proposed Carry Skip Adder

B. Ripple Carry Adder

Ripple carry adder is a form of digital adder circuit. A ripple carry adder is a combination of n-bit full adder connected in series. Every bit addition in ripple carry adder waits for the carry bit from the bit addition before it. The function of a full adder is to add two consecutive bits and carry is shown on the next bit [5]. The carry output of each full adder in a series is connected to the carry input of the subsequent full adder in the sequence to form a ripple carry adder. The way the carry output from each complete adder "ripples" across to the subsequent adder in the chain is where "ripple carry" originates.

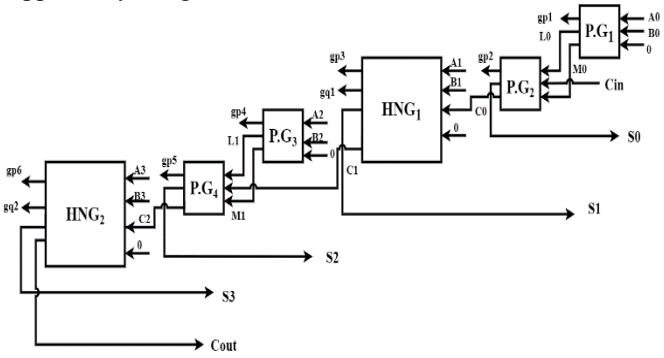

Fig. 8 Proposed Ripple Carry Adder

In the Ripple carry adder four P.G (Peres Gate) and two HNG gate are used. As, one input is made as '0', in this paper Peres gate always act as a AND gate. The two HNG gates act as a full adder. PG_1 and PG_2, PG_3 AND PG_4 both combine to form a full adder. The L_0, M_0 outputs of PG_1 are taken as inputs in PG_2, where A_0, B_0 are inputs of PG_1 and third input of PG_1 is made to '0'. The gate produces a garbage output 'gp_1'. PG_2 takes 'C_{in}' as a third input, resulting in a garbage output 'gp_2' and it produces an output sum termed as 'S_0' and the carry 'C_0' is carried onto the HNG_1 as input along with A_0, B_0. The fourth input is made to "0". HNG_1 produces two garbage output, 'C_1' as carry and sum 'S_1'. Similarly, the carry bit of PG_4 produces an output sum 'S_2' and HNG_2 produces two

garbage output, and it produces a sum 'S_3' and 'C_{out}'. In this circuit the total number of garbage output is 8, ancilla input is 4 and quantum cost is reduced to 28 using four PG (Peres Gate) and two HNG gate whose individual quantum cost are '4' and '6' respectively.

C. Carry Save Adder

Carry Save Adder performs binary addition and is a part of digital adder circuit. Carry save adder does not produce "sum" and "carry" for every bit of addition instead it saves the "carry" for each bit of addition and carry ahead until the last bit of the process of addition. Carry save adder produces two outputs "sum" and "carry". In this paper, carry save adder is made using only PG (Peres gate). Carry save adder also reduces propagation delay unlike ripple carry adder.

The proposed design helps digital circuits to give high performance and it also minimizes power. The two Peres gate 'PG_1' and 'PG_2' and 'PG_7' and 'PG_8' act as a full adder. The L_0, M_0 outputs of PG_1 are taken as inputs in PG_2, where A_0, B_0 are inputs of PG_1 and third input of PG_1 is made to '0'. The gate produces a garbage output 'G_0'. PG_2 takes 'C_{in}' as a third input, resulting in a garbage output 'G_1' and it produces an output sum termed as 'S_0' and the carry 'C_0' is carried onto the next PG_6 as input. Similarly, all the rest PG (Peres gate) carries out operations of 'sum' and 'carry' and produces outputs of sum 'S_1', 'S_2', 'S_3'. 'PG_{11}' takes third input as '0' and it produces output 'SUM' and 'C_{out}' of the entire carry save adder. The quantum cost of the entire circuit is '44', garbage output is '12' and ancilla input is '8'.

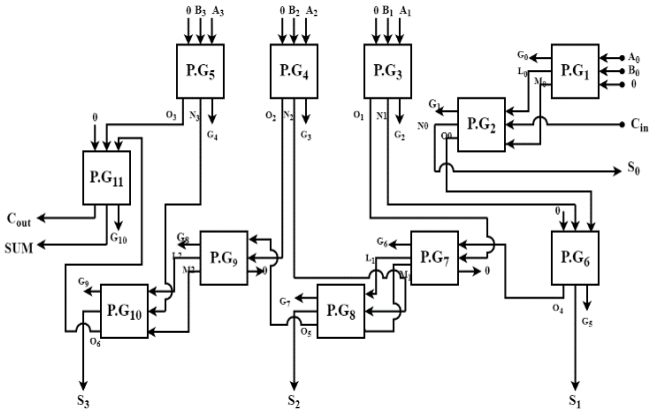

Fig. 9 Proposed Carry save Adder

D. Carry Select Adder

The carry select adder is used for binary addition. It uses parallelism to get values. It is basically a combination of two ripple carry adders. The inputs are first duplicated by the CSA and then moved forward to each adder unit. It assumes various carry input values and computes two sets of sums and carry outputs simultaneously for each adder. The Fredkin gate acts as a multiplexer which chooses the right answer depending on the actual carry in value after both adders have finished their calculations, sum is generated. In this paper, a carry select adder is made using 8 HNG Gate and 5 Fredkin Gate. In this circuit the fourth input is made to '0' and Cin varies from '0' for the first four HNG Gate and '1' for the next four HNG Gates. The output of HNG_1 is carried next to get the HNG_5, reducing its garbage output. The Fredkin gate acts as a multiplexer whereas HNG Gate acts as a full address when one of the inputs is made to '0'. The Fredkin Gate produces sums as 'S_0', 'S_1', 'S_2', 'S_3' and its 'carry' is carried forward. The Gate 'FDG_5' acts as a multiplexer and it computes output as 'C_{out}' from its third output terminal.

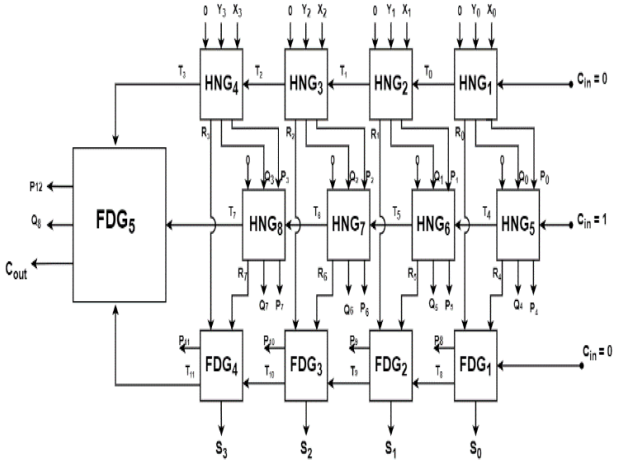

Fig. 10 Proposed Carry Select Adder

V. Simulation and Analysis

The simulation of proposed design has been done using Xilinx Vivado HLS version 2018.2. EDA tools. The paper deals with the simulation of various types of complex adder circuits.

Fig. 11. Simulated output wave of proposed carry skip adder where a=1010, b=1010, c_{in}=0000

Fig. 12. Simulated output wave of proposed ripple carry adder where a=1010, b=1010, c_{in}=0000

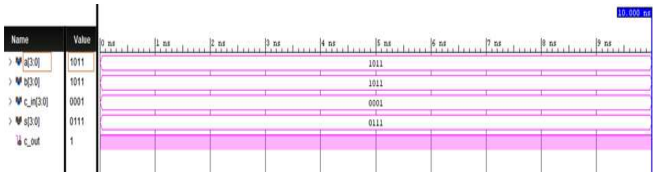

Fig. 13. Simulated output wave of proposed carry save adder where a=1011, b=1011, c_{in}=0001

Fig. 14. Simulated output wave of proposed carry select adder where x=1011, y=1011

Fig.15 and Fig.16 Represents the comparison with existing designs, the comparison shows that the proposed reversible logic–based adders achieve notable improvements over existing designs.

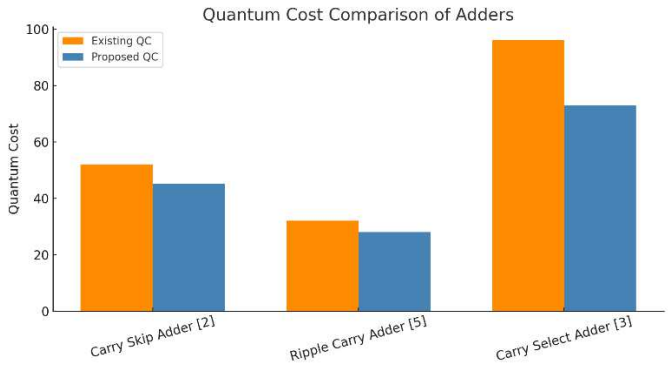

Fig. 15 Quantum cost comparison of proposed reversible adders with existing designs [2], [5], [3].

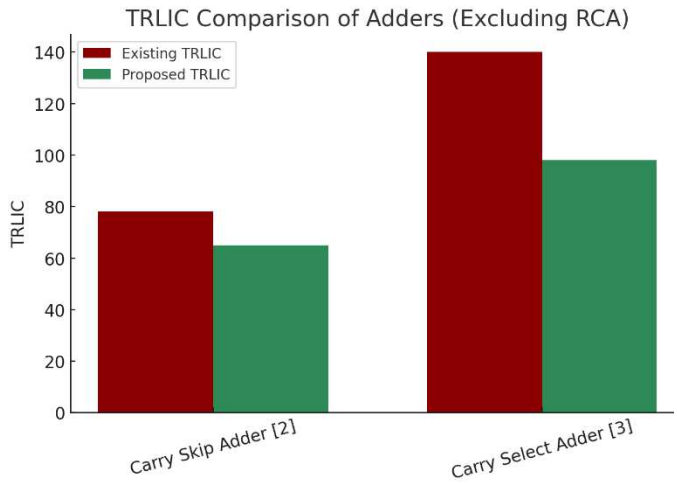

Fig.16 TRLIC comparison of proposed reversible adders with existing designs [2], [3]

VI. CONCLUSION

This work demonstrates the design of efficient hybrid adder architectures using reversible logic. By systematically reducing quantum cost, garbage outputs, and ancillary inputs, the proposed designs achieve superior performance over conventional counterparts. Comparative results confirm improvements in scalability, energy efficiency, and thermal performance, underscoring the practicality of reversible logic for next-generation arithmetic circuits. The optimized designs not only advance low-power VLSI systems but also provide a foundation for quantum computing applications where resource efficiency and reversibility are paramount. Future research may focus on integrating these reversible adders into larger arithmetic and cryptographic architectures, further enhancing their applicability in real-world computing systems.

REFERENCES

[1] T. SaiTeja, S. Srinidhi, P. Santosh, and R. Arun Sekar, "Implementation of Adders using Reversible Logic Gates," *International Journal of Engineering and Information Systems (IJEAIS)*, ISSN: 2643-640X, vol. 4, Issue 4, pp. 16–27, Apr. 2020.

[2] Purna Ramesh Addanki. (2019). Implementation of Low Power Carry Skip Adder using Reversible Logic. International Journal of Recent Technology and Engineering. 8. 2825-2832. 10.35940/ijrte.C5212.098319.

[3] R M, Bommi & S. Selvakumar Raja, Dr. (2019). A novel design of low-power reversible carry selects adder employing MPFA. International Journal of Engineering & Technology. 7. 4780-4784. 10.14419/ijet.v7i4.23138.

[4] P. S. K. Reddy and G. Saini, "Design of Carry Select Adder with Online Testability Using Reversible Gates," *2019 4th International Conference on Recent Trends on Electronics, Information, Communication & Technology (RTEICT)*, Bangalore, India, 2019, pp. 486-490, doi: 10.1109/RTEICT46194.2019.9016873.

[5] N. Somani, C. Chaudhary and S. Yadav, "Reversible adder design for ripple carry and carry look ahead (4, 8, 16, 32-bit)," *2016 International Conference on Computing, Communication and Automation (ICCCA)*, Greater Noida, India, 2016, pp. 1387-1392, doi: 10.1109/CCAA.2016.7813935.

[6] Gowthami P and RVS Satyanarayana, "Design of Digital Adder Using Reversible Logic," *Gowthami P Int. Journal of Engineering Research and Applications*, Vol. 6, Issue 2, (Part - 1), ISSN: 2248-9622, pp.53-57, Feb. 2016.

[7] V. S. P. Nayak, N. Ramchander, R. S. Reddy, T. H. S. P. Redy and M. S. Reddy, "Analysis and design of low-power reversible carry select adder using D-latch," *2016 IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT)*, Bangalore, India, 2016, pp. 1917-1920, doi: 10.1109/RTEICT.2016.7808169.

[8] A. Bose and H. M. H. Babu, "Optimized designs of reversible fault tolerant BCD adder and fault tolerant reversible carry skip BCD adder," *2015 18th International Conference on Computer and Information Technology (ICCIT)*, Dhaka, Bangladesh, 2015, pp. 202-207, doi: 10.1109/ICCITechn.2015.7488068.

[9] Tarunkumar C. Lad and Patel Fenil S., "VHDL Implementation of 4-Bit Full Adder Using Reversible Logic Gates," *IJSRD-International Journal for Scientific Research & Development*, vol. 1, no. 10, pp. 2279–2283, Jan. 2014, ISSN (online): 2321-0613.

[10] R. M. Swaraj, K. K. Arun and R. K. Srinivas, "Reversible implementation of novel multiply accumulate (MAC) unit," *2012 International Conference on Communication, Information & Computing Technology (ICCICT)*, Mumbai, India, 2012, pp. 1-5, doi: 10.1109/ICCICT.2012.6398218.

[11] M. Praveena and K. Thanushkodi, "Survey and evaluation of various reversible carry skip BCD adders," *2012 IEEE International Conference on Computational Intelligence and Computing Research*, Coimbatore, India, 2012, pp. 1-5, doi: 10.1109/ICCIC.2012.6510244.

[12] S. S. Chiwande and P. K. Dakhole, "VLSI design of power efficient Carry Skip Adder using TSG & Fredkin reversible gate," *2012 International Conference on Devices, Circuits and Systems (ICDCS)*, Coimbatore, India, 2012, pp. 370-373, doi: 10.1109/ICDCSyst.2012.6188788.

[13] M. S. Islam, M. M. Rahman, Z. Begum and M. Z. Hafiz, "Fault tolerant reversible logic synthesis: Carry look-ahead and carry-skip adders," *2009 International Conference on Advances in Computational Tools for Engineering Applications*, Beirut, Lebanon, 2009, pp. 396-401, doi: 10.1109/ACTEA.2009.5227871.

[14] A. K. Biswas, M. M. Hasan, M. Hasan, A. R. Chowdhury and H. M. H. Babu, "A Novel Approach to Design BCD Adder and Carry Skip BCD Adder," *21st International Conference on VLSI Design (VLSID 2008)*, Hyderabad, India, 2008, pp. 566-571, doi: 10.1109/VLSI.2008.37.

[15] S. Dasgupta, S. Pandey, D. Roy, A. Maity, A. Sinha and M. L. Saha, "Design and Implementation of an Efficient Quantum Cost Optimized Adder Using Reversible Logic Gates," *2025 8th International Conference on Electronics, Materials Engineering & Nano-Technology (IEMENTech)*, Kolkata, India, 2025, pp. 1-6, doi: 10.1109/IEMENTech65115.2025.10959433.