Chakra-1: Ultra-Lightweight Hybrid Cipher Architecture for Next Generation IoT Security

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***Abstract*—The prevalence of Internet of Things (IoT) in fundamental sectors such as health services, industrial automation, and smart infrastructure has intensified the demand of lightweight cryptography solutions with high security that operate with a very strict resource constraint. The current paper presents Chakra-1, a hybrid block cipher architecture which is extremely lightweight and combines the Substitution-Permutation Network (SPN) and Feistel models. A 64-bit data block is encrypted by the design with 128-bit master key by means of a bit-jumbling permutation as an alternative to traditional S-boxes to provide diffusion at the lowest hardware cost. A key scheduling algorithm without gates is proposed to avoid extra hardware expenses. The proposed cipher features a notably smaller hardware footprint of 448 Gate Equivalents (GE), extremely low power usage of 2.390 µW, and a minimal delay of just 3.374 ns when implemented using 90 nm technology. The proposed block cipher successfully completed all 15 evaluations from the NIST SP 800-22 suite using 1 billion cipher text outputs, demonstrating strong statistical randomness. Analysis of its performance reveals that it is more efficient than existing lightweight ciphers in terms of area, delay, and energy usage.**

Keywords— Lightweight cryptography, Hybrid block cipher, IoT Security, SPN- Feistel architecture, Low power encryption

I. Introduction and Related Works

In this era of advancing technologies, various different devices are linked and connected to each other, wireless through the internet, to build a smarter ecosystem of devices that will make tasks simpler, thus causing an advent of IoT. A question of privacy and security arises as the internet is used by the physical devices for interaction with each other [1]. In order to secure the ecosystem of devices through IoT a need for encryption of data comes into play. Lightweight cryptography is introduced to deal with the security level of the IoT constrained devices as the conventional cryptographic algorithms are unsuitable for IoT constrained devices [2]. NIST has provided certain criteria that are required to be fulfilled for making the cryptography algorithms lightweight which is suitable for IoT constrained overcoming the issue of space constraints whereas maintaining an efficient and smooth performance. These algorithms are perfect for applications such as embedded devices, tags with RFID, smart cards, and wireless sensors since they are especially designed to provide adequate security with minimal computational and hardware overheads [3].

In cryptography algorithms to make the exchange of information secure, a public or private key is used along with the plain text to obtain the cipher text in encrypted form. Primarily either of the two types of keys is used in any cryptography algorithms which are – symmetric key or asymmetric key. With the help of symmetric key, block cipher [4] or stream cipher can be generated of which block ciphers are more efficient and provide better performance [5]. In earlier days, Advanced Encryption Standard (AES) [6] and Data Encryption Standard (DES) [7] were used in which SPN and Feistel structure were used as the structure for algorithms respectively. SPN structure in the AES has multiple rounds that help in providing robust security but it cannot be used in the modern IoT constrained devices as it had greater power consumption and the gate area were rather high. The Feistel structure in DES was lighter in comparison of the AES but it was susceptible to brute force attack because of short key length. Thus, they were replaced by lightweight cryptography which is appropriate and suitable for IoT constrained devices. In the latest lightweight cryptography algorithm, the ciphers like - ANU [8], RECTANGLE [9], GIFT [10], SIMON and SPECK [11], ACT [12], BORON [13], and PICCOLO [14] are designed on the basis of SPN and Feistel structure. The SPN and Feistel structure are combined to form new cipher designs which are lightweight as well as provide robust security. They have lesser number of rounds than the AES but larger key size than DES making the newer cipher both robust and lightweight. This improvement in the cipher design over the conventional cryptographic algorithms has helped in the designing of lightweight block cipher which can be used in the IoT constrained devices. Furthermore, the landscape of lightweight ciphers has become even more varied with the introduction of new design philosophies including the utilization of ARX (Addition, Rotation, and XOR) structures and tweakable block ciphers [15].

Despite the presence of numerous cryptographic block cipher algorithms, a large amount of research work on lightweight cryptography needs to be done, as most of the existing algorithms possess some limitations and challenges that must

be overcome for efficient implementation in IoT-constrained devices. A novel cryptographic block cipher which is ultra-lightweight in nature has been proposed in this paper for IoT devices with resource-constrained by combining the SPN and Feistel structures to provide robust security while consuming less gate equivalent area and power.

II. Construction of Proposed Block Cipher

This work introduces a newly designed ultra-lightweight block cipher specifically aimed at IoT devices with low power, such as compact sensors, smart cards, and RFID systems, while still ensuring a satisfactory level of security. It has a unique hybrid design which combines both SPN and Feistel-based encryption designs with the ability to operate using a data block of 64-bit and a key size of 128 bits. This design does not have S Boxes unlike in traditional block ciphers that are used to provide confusion and diffusion in encryption. Rather, the bit diffusion jumbling process is applied during each round of iteration through bit permutation which essentially repeats the role of substitution boxes. A complete gateless key schedule algorithm is used to enhance security which does not require any additional hardware.

It is a block cipher which uses 64-bit plaintext blocks and 128-bit key, so it can be used in very light security implementations. It is a Feistel network that is created by combining substitution and permutation layers, which consists of eight encryption rounds. The encryption and decryption algorithms with detailed description is given in the following section.

A. Main Algorithm

The plaintext of 64-bit is split into four 16-bit plaintext blocks. These blocks may be referred to as: P1, P2, P3, P4.

A total of 8 encryption rounds is performed. Each round uses one round key (K_1 to K_8) and four F (jumbling) blocks. For each round (i = 1 to 8):

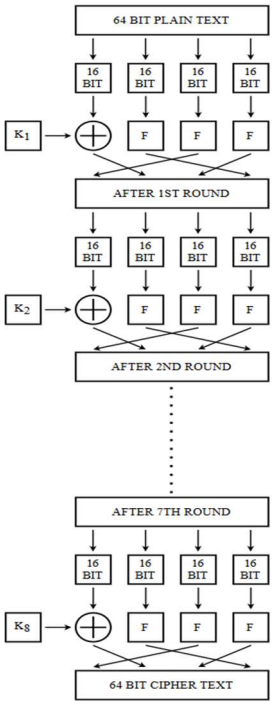


Fig. 1 Encryption Process of Proposed Cipher

Step 1: Take the first 16-bit block P1 and XOR it with the round key K_i.

Step 2: The result of XOR is passed through the F Block (permutation).

Step 3: Pass blocks P2, P3, and P4 through the F Block directly.

Step 4: Perform inter-block permutation between all four blocks as per the defined wiring scheme in the architecture diagram.

Step 5: The output becomes the new set of P1, P2, P3, P4 for the next round.

This process continues for 8 rounds, updating all blocks through XOR, F Block, and inter-permutation in each round. After the final (8^{th}) round, the 4 processed 16-bit blocks are concatenated to form the final 64-bit cipher text.

B. Jumbler Block

One input of 16 bits x[n] and Output of 16 bits y[n].

Y[n]=x[15], x[13], x[11], x[9], x[7], x[5], x[3], x[1], x[14], x[12], x[10], x[8], x[6], x[4], x[2], x[0]

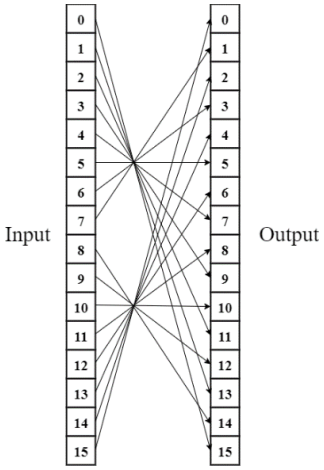


Fig. 2. F Block (Jumbler Block)

C. Key Generation Algorithm

A secret key of 128-bit is used to derive 8 round keys (K_1 to K_8), each of 16 bits.

Steps:

Eight 16-bit sub-blocks are formed by dividing the 128-bit key. Each 16-bit block is represented as a 4x4 matrix.

Each matrix is passed through a rotation operation, which scrambles the bits to enhance complexity. The rotation operation consists of eight step – row shift and column shift alternatively.

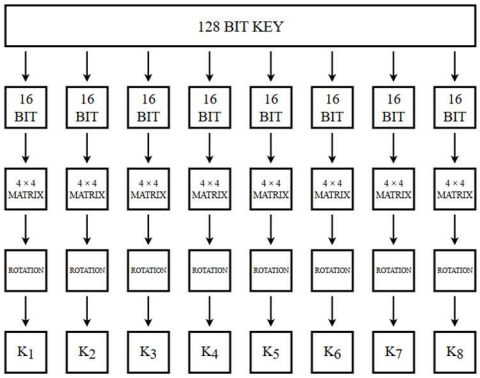


Fig. 3 Key Generation

In the row shift operation, the first row is shifted to its right (0,1,2,3) > (3,0,1,2) the remaining matrix remains unchanged.

In the column shift operation, the column row is shifted to its top (0,4,8,12) -> (12,0,4,8) the remaining matrix remains unchanged.

The output of each rotation gives a round key of 16-bit: K_1, K_2, K_3, K_4, K_5, K_6, K_7, K_8.

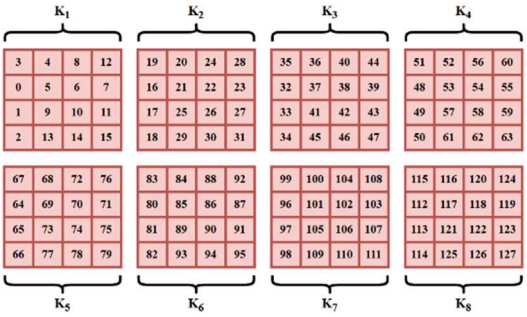


Fig. 4 Key Matrix Block

D. Encryption Procedure

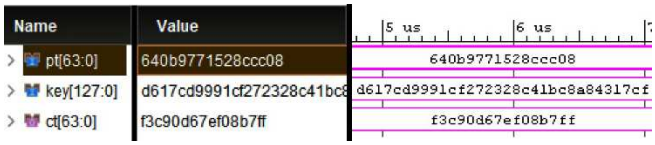
The method proposed uses jumbling of bits, matrix manipulations and simple logical XOR operations. Consequently, the data can only be decrypted by the authorized users to use it. The revealed system operates using 64 bits of plaintext data and was made as lightweight as possible. To enable this, the huge data block will be divided into several 16-bit segments with each segment being handled by different data channel. The same process is also repeated with other blocks of data. In the obtained output, the results of all the processed data block are added to obtain the encrypted data. The primary key is split into eight 16-bit sub keys used in several rounds of encryption. This will guarantee the method provides a high quality of performance on resource-restricted devices. The proposed encryption algorithm uses low power and needs minimal memory as well as low storage space.

E. Decryption

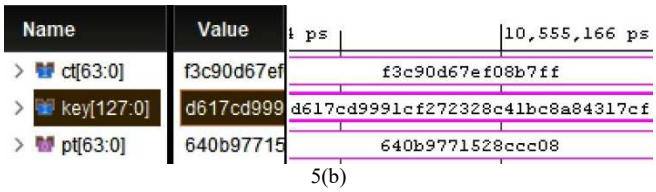
For decryption of data, the encryption process will be performed in the reverse sequence of the rounds that are used in encryption. The 16-bit blocks of cipher text are subjected to inverse inter-block permutations, inverse F block operations and XOR operations with the corresponding round keys in reverse order (K8 to K1) to basically reassemble the original 64-bit plaintext.

III. Simulation and FPGA Based Implementation

This section contains the results of the proposed architecture of an ultra-lightweight block cipher developed with the help of Verilog HDL. To confirm the performance of the cipher, all the simulations were performed in Xilinx Vivado 2018.2 web pack version where the implementation was done on the Artix-7 Xilinx FPGA.



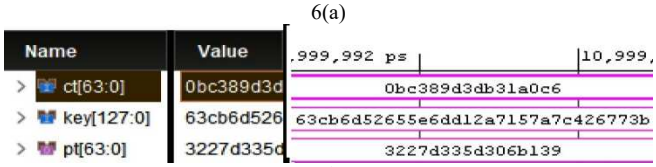
5(a)



5(b)

Fig. 5 (a), 5(b) Simulated Output of Test Case 1

6(a)



6(b)

Fig. 6 (a), 6(b) Simulated Output of Test Case 2

Figures 5(a) and 5(b) show an encryption and decryption process of test case 1 and Figures 6(a) and 6(b) represent an encryption and decryption process of test case 2. Table I represents the test cases, detailing the plaintext and keys utilized in the simulation process within the Xilinx Vivado tool. The test cases are presented in hexadecimal bit format.

TABLE I. Test Cases

Serial No.	Plain Text	Key	Cipher Text
Test Case 1	640b9771528ccc08	d617cd9991cf272328c41bc8a84317cf	f3c90d67ef08b7ff
Test Case 2	3227d335d306b139	63cb6d52655e6dd12a7157a7c426773b	0bc389d3db31a0c6

IV. Performance Evaluation

The newly developed method has attained a remarkably low equivalent gate count of just 448 GE and demonstrates impressive speed with a minimal computational time of 3.374 ns, alongside ultra-low power consumption of 2.390 µW when evaluated in Cadence Genus using Gpdk 90 nm process technology. Furthermore, it was synthesized on a Virtex 5 (xc5vlx30-3-ff324 - 65 nm) FPGA board utilizing Xilinx ISE 14.7. Table II displays the comparative analysis with the existing algorithms that were created utilizing either the SPN or Feistel architecture.

TABLE II. Comparison of Lightweight Block Cipher Algorithms

Ciphers	Block Size (Bit)	Key Size (Bit)	Structure	Area (GE)
PROPOSED	64	128	SPN, FEISTEL	448
SIMON[11]	32	64	FEISTEL	523
SPECK[11]	32	64	FEISTEL	580
GOST[30]	64	256	FEISTEL	651
PICCOLO[14]	64	80	FEISTEL	683
ANU[8]	64	80	FEISTEL	1015
QTL[29]	64	64	SPN, FEISTEL	1026
TEA[28]	64	128	FEISTEL	1140

ACT[12]	64	80	SPN	1481
TWINE[27]	64	80	FEISTEL	1503
MIDORI[26]	64	128	SPN	1542
SAND[25]	128	128	FEISTEL	1563
PRESENT[24]	64	80	SPN	1570
RECTANGLE[9]	64	80	SPN	1599.5
LOONG[23]	64	128	SPN	1766
SFN[22]	64	96	SPN, FEISTEL	1876.04
BORON[13]	64	128	SPN	1939
mCRYPTON[21]	64	64	SPN	2420
CLEFIA[20]	39	128	FEISTEL	2488
KLEIN[19]	64	80	SPN	2629
HIGHT[18]	64	128	FEISTEL	3048
AES[17]	8	128	SPN	3100
LED[15]	64	128	SPN	3407
PRINCE[16]	64	128	SPN	3491

Although not all published cipher research has provided details on all parameters—specifically area, delay, and power—we have compared the delay and power of existing algorithms that have been reported. Figures 7 and 8 illustrate the comparison of delay and power with the existing block cipher algorithm.

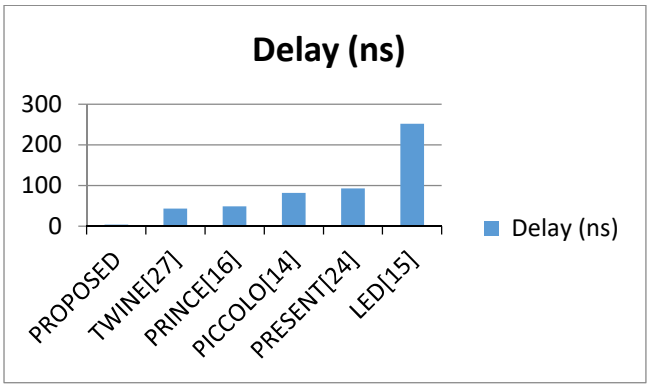


Fig. 7 Comparison of Delay with Existing Cipher

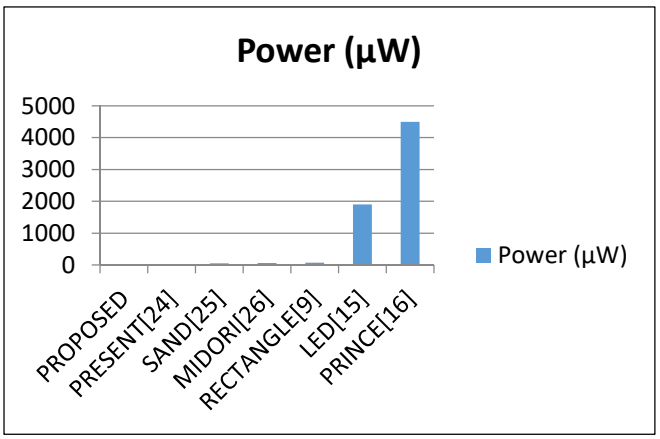


Fig. 8 Comparison of Power with Existing Cipher

NIST SP 800-22 consists of 15 standard tests typically employed to detect non-random sequences by examining specific patterns. For the analysis, 100 bit streams were produced using the proposed block cipher encryption algorithm. The proposed cipher mechanism is assessed for randomness through the 15 statistical tests provided by the National Institute of Standards and Technology (NIST) in the SP 800-22 suite. The testing was conducted with 1 billion cipher text outputs. All tests have been completed successfully. Table III displays the NIST test outcomes with their corresponding passed values.

TABLE III. NIST SP 800-22 RANDOM TEST ANALYSIS

NIST Test	P - Value	Results
Frequency	0.574903	Pass
Block Frequency	0.026948	Pass
Cumulative Sums	0.816537	Pass
Runs	0.637119	Pass
Longest Run	0.514124	Pass
Rank	0.455937	Pass
FFT	0.096578	Pass
Non-Overlapping Template	0.983453	Pass
Overlapping Template	0.514124	Pass
Universal	0.534146	Pass
Approximate Entropy	0.779188	Pass
Random Excursions	0.971699	Pass
Random Excursions Variant	0.911413	Pass
Serial	0.911413	Pass
Linear Complexity	0.334538	Pass

V. CONCLUSION

The design and development of Chakra-1 address the urgent need to have effective and safe encryption in IoT-like settings with limited available resources. The NIST SP 800-22 test suite verified the high level of statistical randomness in the algorithm as all 15 tests were successfully passed with a dataset of 1 billion cipher text outputs. The experimental results reveal that Chakra-1 has a 448 GE area, very low power consumption, and low delay, which is suitable in the low-power, memory-limited IoT devices. This, along with its better comparative performance values, highlights the possibility of it as an effective solution in the future of implementing IoT security. Future studies will focus on advanced cryptanalysis, integration of authenticated encryption and resistance against post quantum attacks.

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