Quantum-Ready ALU: Optimized Design Using Reversible Logic with RTL Design and FPGA Implementation

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***Abstract*— Reversible logic provides a foundation for next-generation computing systems, particularly in quantum and emerging nanotechnology-based architectures. Unlike conventional logic, reversible gates preserve information and support backward computation, making them crucial for designing quantum circuits. This paper introduces a reversible Arithmetic and Logic Unit (ALU) that performs eight fundamental operations—AND, OR, NOT, XOR, addition, subtraction, increment, and decrement—using Fredkin, Peres, TR, and modified Fredkin gates. A dedicated control unit manages operation selection, ensuring functional flexibility and circuit efficiency. The proposed design achieves significant improvements by minimizing ancilla inputs, quantum cost and garbage outputs, resulting in a total quantum cost of 71 and contains 16 reversible gates and 14 garbage outputs. The architecture was modeled and verified using Xilinx Vivado HLS and ISE 14.7, and implemented on the Nexys A7 (Artix-7) FPGA platform. Comparative analysis demonstrates better efficiency than existing reversible ALU designs, establishing the proposed circuit as a strong candidate for quantum computing and other advanced computing paradigms.**

Keywords*— *Reversible logic, ALU, RTL Design, FPGA, VLSI

I. Introduction and Related Works

Reversible logic gates play an integral role in today's Very Large-Scale Integration (VLSI) designs [1]. They do not lose data and consume less power in computation, offering a better alternative to traditional gates [2]. As compared to usual gates, say AND, OR, and NOT, whose outputs can lose information, reversible gates contain equal numbers of outputs and inputs, i.e., there is no loss of data during computation. As per Landauer's principle, if one information bit is lost in an ordinary circuit, it produces in heat an amount of kTln2 joules, wherein T denotes absolute temperature and k is Boltzmann's constant [3]. Since reversible logic incurs no loss of bits, Bennett demonstrated that computations performed under it can avoid this loss of energy [3], [4].

These reversible gates have one-to-one mappings as their foundation, and any different input pattern results in one new, distinct output pattern, allowing inevitability [5]. Due to this one-to-one correspondence, back computation can be achieved, which minimizes energy loss as the original inputs can be retrieved from the outputs [1], [6]. These characteristics, with reversible logic, are highly favorable to small, low-energy VLSI as well as quantum computing [7].
The CPU (Central Processing Unit) contains a digital circuit unit known as the ALU (Arithmetic and Logical Unit), which is crucial for performing various arithmetic and logical functions within the circuit, such as addition, AND, subtraction and OR operations. The ALU receives data and instructions from the Control Unit and uses digital logic gates to perform specific arithmetic or logical operations. The result is then stored in a register or other components in the CPU. Power dissipation measurement in conventional logic is critical. As mentioned by Landauer in his paper, the loss of 1-bit information causes an energy loss of KT*ln2 joules, where T denotes the temperature and K is defined as Boltzmann's constant. As heat is increased more data or information is lost in case of a combinational circuit. But, after losing information, it cannot be restored. There is a direct connection between the number of bits lost and power consumption, so with increase in quantum cost and gate count can cause more power loss [12]. A reversible logical gate can be used to overcome this loss due to energy dissipation. Bennett, in his paper, proposed that by utilizing the concept of reversibility, reversible computers can dissipate a smaller amount of heat, thereby increasing the circuit's utility.[7]. In this paper the novel Reversible gates and an Arithmetic and Logical Unit are proposed and applied in the gates in collaboration with a Control Unit. The Arithmetic part does the addition, subtraction, increment and decrement but the logical part is concerned with the AND, OR, NOT and XOR functions. The Control Unit allows us to choose which operation to perform. The Reversible Logical gate is used in

2026 9th International Conference on Electronics, Materials Engineering & Nano-Technology (IEMENTech) | 979-8-3315-6339-4/26/$31.00 ©2026 IEEE | DOI: 10.1109/IEMENTECH202669403.2026.11434363

low-power CMOS, DNA computing, Quantum Computing, and optical information processing.

As mentioned, increase in quantum cost and TRLIC can affect the loss of energy. In recent years, Ravi L S et al. [1] have designed an ALU using reversible gates, which can be used for quantum computing. Despite its implementation in quantum computing, the circuit requires more power due to quantum cost and TRLIC. Zhijin Guan et al. [6] have designed the ALU using reversible gates, which can be used for quantum computing. Their design, innovative as it is, leads to a high quantum cost and a high number of gate counts. In the circuit proposed in this paper, the design targets to minimize ancilla input, quantum cost, and garbage outputs.

II. Reversible Logic Gates Overview

The logic gates of reversible are circuits which have 'n' input and 'n' output such that each input is mapped with the corresponding output. The inputs have the ability to retrace the outputs and vice versa. The key parameters of Reversible logic gates are:

- Ancilla inputs/Constant input: Which are the inputs that are kept constant (for e.g., 0 and 1) to synthesize desired outputs.
- Garbage output: Which are the outputs that is not further utilized.
- Quantum Cost: Is the cost of the circuit in terms of primitive gates.

A. FREDKIN GATE

Fredkin Gate is a reversible gate in which there are three inputs and three outputs depicted. Here, the inputs are denoted by X, Y and Z and the outputs denoted by S, T and U. The fig 1 indicates the outputs of the gate. It has a quantum cost of 5.

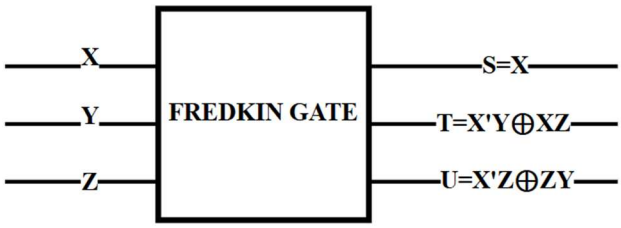

Fig.1 Fredkin Gate [12]

B. PERES GATE

In Peres Gate, 3 inputs are entered and 3 outputs are given out. X,Y and Z are the three inputs and S,T and U are the three outputs. The outputs of the gate is given in fig 2. It has a quantum cost of 4.

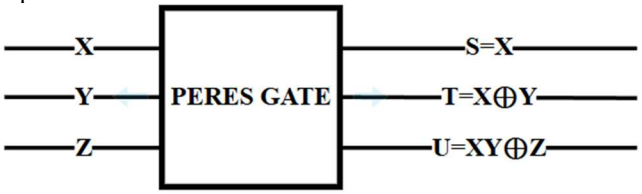

Fig.2 Peres Gate [12]

C. TR GATE

TR Gate is basically a reversible gate which contain 3 inputs and 3 outputs. The three inputs are X, Y and Z and their outputs are S, T and U. The outputs of the gate is given in fig 3. The quantum cost of TR Gate is 4.

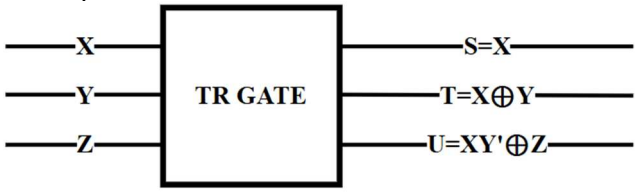

Fig.3 TR Gate [12]

D. MODIFIED FREDKIN GATE

Modified Fredkin Gate is a reversible gate which takes three inputs and three outputs. It has three inputs X, Y and Z and three outputs S, T and U.

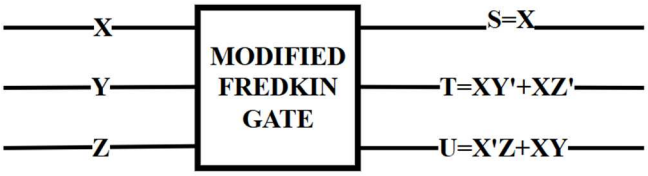

Fig.4 Modified Fredkin Gate [12]

III. Proposed Methodology

The methodology focuses on designing an Arithmetic and Logic Unit (ALU) capable of performing eight fundamental operations, divided into four logical and four arithmetic functions. Initially, a conventional ALU was implemented using basic logic gates to serve as a reference model. Subsequently, an optimized ALU was developed using reversible logic gates, aimed at reducing quantum cost, ancilla inputs, and garbage outputs. Finally, the proposed design was modeled at the RTL level and validated through FPGA implementation to ensure its practical applicability.

A. ALU Using Basic Logic Gates

The proposed ALU architecture does 8 operations (4 logical and 4 arithmetic) of the ALU presented in fig.5. The first operation of the logical unit is the OR operation which takes two input A and B respectively and passes them through an OR gate. The output is thus A+B. The output is then connected to the 8:1 MUX. This operation occurs when the value of the select lines are all 1. The second operation of the logical unit is the NOT operation which takes only one input i.e. A and gets passed through a NOT gate to receive the complement value of A as the output which is again connected to the 8:1 MUX. This operation occurs when the select line conditions are S_2=1, S_1=1 and S_0=0. The third logical operation is the XOR operation where both the inputs A and B are passed through a XOR gate to get the output as A XOR B Boolean expression which goes to the 8:1 MUX as input. This operation occurs when the select line conditions are S_2=1, S_1=0 and S_0=1. The last logical operation in the proposed ALU design is the AND operation where the inputs A and B gets passed through an AND gate which gives an output of AB and is connected with the 8:1 MUX. This operation is selected when the values of the select lines are 1, 0 and 0 respectively.

The first arithmetic unit operation is sum. Here, A and B enters a half adder as inputs. The first output is the addition result of A and B, which goes into the 8:1 MUX and the second output is the carry, which goes into a 4:1 MUX. For this condition to work, the select line conditions for the 8:1

MUX will be 0, 1 and 1 respectively. The second arithmetic operation is increment of A by 1.

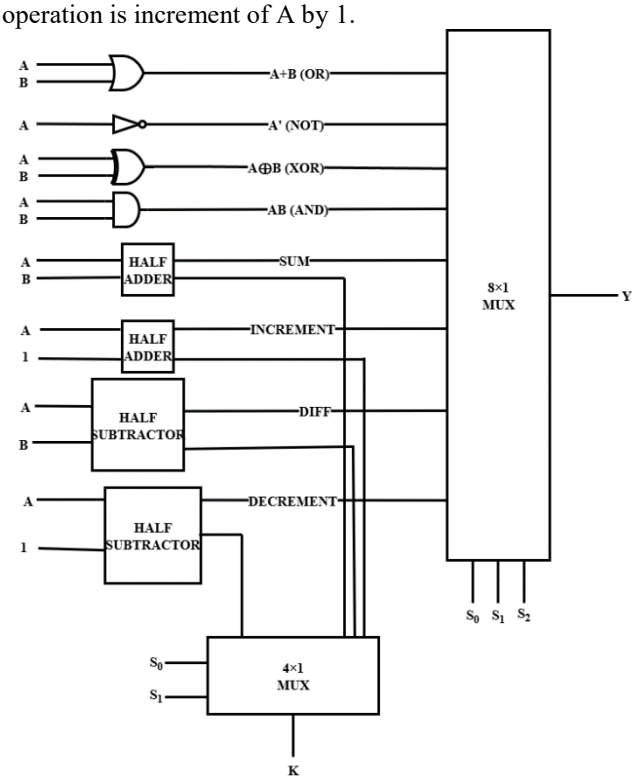

Fig.5 Proposed ALU architecture Using Basic Gates

This is done by taking A and a constant input 1 as inputs and passed through a half adder. The A+1 part goes to the 8:1 MUX and the carry part goes to the 4:1 MUX. The select lines for this is S_2=0, S_1=1and S_0=0. The third arithmetic operation is difference where A and B, two inputs enter a half subtractor and the first output comes out to be A-B which goes into the 8:1 MUX and the second output which is the borrow part goes into the 4:1 MUX. This operation takes place when the select lines are 0, 0 and 1 respectively. The last arithmetic operation is decrement where the two inputs A and 1 are entered into another half subtractor and the output comes out to be A-1 which goes into the 8:1 MUX and the borrow part which goes to the 4:1 MUX. The select lines for this is S_2=0, S_1=0 and S_0=0. According to the select line conditions, the desired operation takes place and only one output Y comes out from the 8:1 MUX. Similarly for all the carries and borrows which goes into the 4:1 MUX, in the arithmetic part, only one output i.e. K comes out according to the conditions of select lines.

B. ALU Using Reversible logic Gates

The proposed model performs eight fundamental operations, comprising four logical (AND, OR, NOT, XOR) and four arithmetic (Addition, Subtraction, Increment, Decrement) functions. Reversible gates were employed to optimize the design by reducing quantum cost, garbage outputs, and ancilla inputs. The logical unit was implemented using Fredkin, Peres gates and Modified Fredkin gates. OR and NOT operations were realized through a Fredkin gate, while XOR and AND operations were achieved using a Peres gate. For the arithmetic unit, Peres gates were utilized for addition and increment operations, whereas TR gates were applied for subtraction and decrement. Modified Fredkin (MF) gates were incorporated as multiplexers to control operation selection within both logical and arithmetic units.

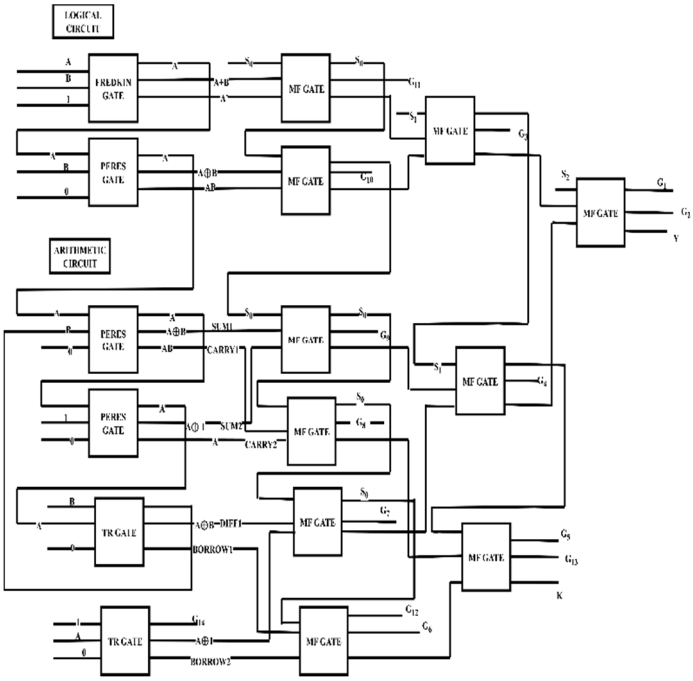

Fig.6 Proposed ALU architecture Using Reversible Gates

The final control unit used select lines to distinguish between logical and arithmetic operations, producing the desired output Y along with a secondary output K.

TABLE 1. OPERATION TABLE OF PROPOSED ARCHITECTURE

SELECT LINES			OUTPUT Z	FUNCTION	UNITS
S_2	S_1	S_0			
1	1	1	A+B	OR	LOGICAL UNIT
1	1	0	A’	NOT (Complement of A)	
1	0	1	A⊕B	XOR	
1	0	0	AB	AND	
0	1	1	A+B	Addition of A and B	ARITHMETIC UNIT
0	1	0	A+1	Increment of A by 1	
0	0	1	A-B	Subtraction of B from A	
0	0	0	A-1	Decrement of A by 1	

The architecture demonstrates an efficient approach to implementing reversible ALUs, ensuring optimized resource utilization while preserving reversibility.

IV. Simulation Results and FPGA Implementation

The simulation of the proposed design was performed using Xilinx Vivado HLS version 2018.2 and Xilinx ISE 14.7 EDA tools, as shown in Table 2, following synthesis with Xilinx ISE 14.7. The delay of the proposed design is obtained as 1.0356 ns. It is observed that 16 reversible gates were used in the proposed design of the ALU. The circuit contains 14 garbage outputs, 2 Constant inputs, and the Quantum cost is 71. The table 2. shows the comparative study and improvements with existing ALU using reversible gates

TABLE 2. COMPARITIVE STUDY WITH EXISTING DESIGN

PARAMETERS	GC	CI	GO	QC	% OF IMPROVEMENT	TRLIC	% OF IMPROVEMENT
PROPOSED	16	2	14	71		87	
[1]	NR*	3	11	90	21.11%	NR*	
[3]	17	16	33	76	6.57%	142	38.73%
[5]	14	3	20	94	24.46%	131	33.58%
[6]	NR*	6	19	104	31.73%	129	32.55%

Fig.7 depicts the simulated output of the proposed circuit. Moreover, Figure 8 shows the RTL design of the circuit proposed in this paper.

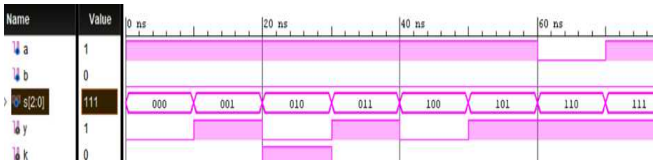

Fig.7 Simulated output wave of proposed ALU

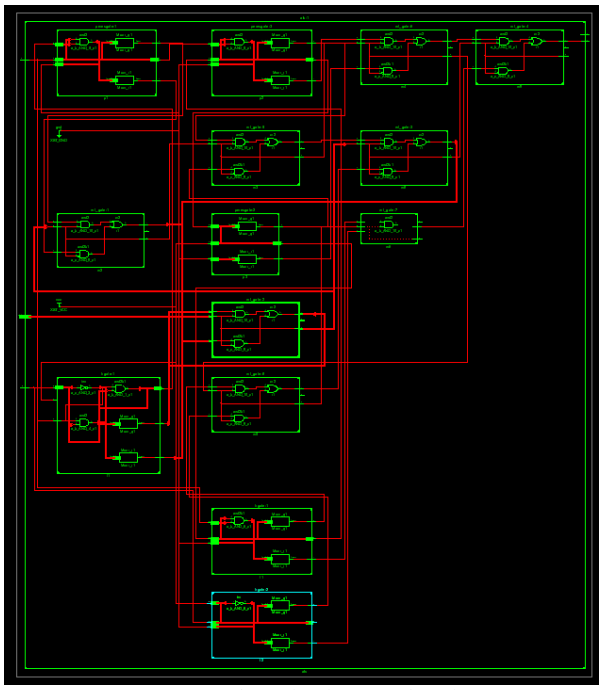

Fig.8 RTL schematic of proposed Design

Figure 8. shows the RTL design of the circuit that is proposed in this work. Figure 9 illustrates the FPGA implementation of the OR operation, where from the top-right corner switches represent the input, and the LEDs represent the output.

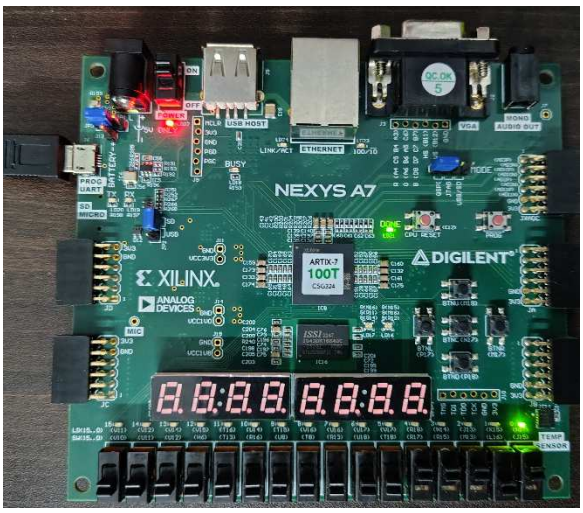

Fig.9 FPGA Implementation of Proposed ALU

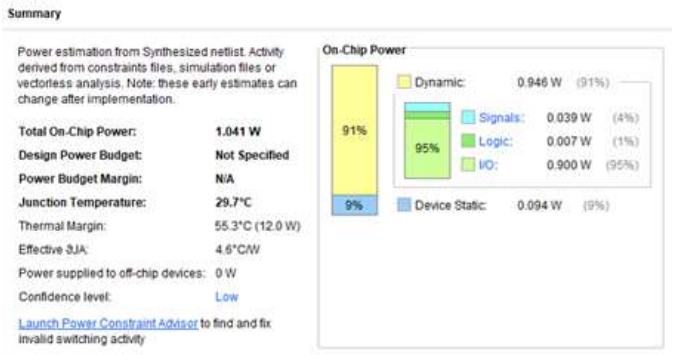

Fig.10 On Chip Power of Proposed ALU unit

FPGA implementation of the proposed architecture has been carried out using NEXYS A7 (Artix 7 series – XC7ACSG324C) FPGA board. Figure 9 illustrates the FPGA implementation of the OR operation, where from the top-right corner switches represent the input, and the LEDs represent the output. Figure 10. Represents the power estimation after synthesis of the proposed design. Using the NEXYS A7 FPGA Board.

V. Conclusion

This paper presents a reversible ALU architecture capable of executing both arithmetic and logical operations efficiently. The design leverages Fredkin, Peres, TR, and modified Fredkin gates to implement eight basic operations while significantly reducing quantum cost, ancilla inputs, and garbage outputs compared to previous approaches. Hardware implementation on an FPGA verified the functionality and practicality of the proposed architecture, with simulation results confirming a delay of 1.0356 ns and effective resource utilization. With its optimized parameters and adaptability, the proposed ALU represents a step toward practical deployment of reversible logic in quantum computing systems and other futuristic computing technologies.

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