A Simplified Quantum Circuit for Addition Using the Lilavati–Bhashkaracharya Method

Rijuparna Chakraborty[1, a)], Mili Sarkar[1, b)], Debabrata Dutta[2, c)]
[1]*Institute of Engineering and Management, Sector-V, Salt Lake, Kolkata -700091*
[2]*Heritage Institute of Technology, East Kolkata Township, Kolkata-700107*

[a)] Corresponding author: rijuparna.chakraborty@iem.edu.in
[b)] mili.sarkar@iem.edu.in
[c)] debabrata.datta@heritageit.edu

Abstract. Quantum computing promises exponential speedups for many classical problems, especially for arithmetic operations. In quantum arithmetic circuits, the adder is the principal operational unit. For executing this addition operation on numbers, we normally start summing from right most digits and gradually shift left with carry. And this method is followed in electronic and quantum circuitry too. Therefore, for n-digit operation we need (n-1) full-adders and one half adder, and these n-parts of the total circuit operates one by one taking n-units of time. Here we present a simplified quantum circuit using Lilavati – Bhashkaracharya Method, which performs the total addition operation of any number of digits using 3-units of time and it requires only half adders. The proposed Lilavati-method based quantum adder offers a blend of historical insight and modern computational efficiency, bridging classical mathematical heritage with cutting-edge quantum technology.

INTRODUCTION

Quantum arithmetic circuits [1-3] are fundamental components in quantum algorithms, particularly those used in cryptography, search operations and optimization [4,5]. Traditionally, n-bit addition in classical and quantum circuits requires (n-1) full adders and one half adder, with carry bits propagating sequentially from the least significant bit to the most significant bit. This paper presents a quantum adder circuit design inspired by the Lilavati – Bhashkaracharya Method [6] which offers an elegant and efficient approach to addition without the need for carry propagation. It describes arithmetic operations such as addition and subtraction in a place-wise manner. Instead of propagating carry from one digit to the next, digits of the same place-values are added independently. The final result is obtained by combining these digit-wise sums along with their respective place-values.

MATHEMATICAL PROCEDURE

The verses that described the method of addition in Lilavati by Bhashkaracharya, indicated that addition or subtraction can be done place-wise and there is no need to perform it from left to right. Rather one should sum up the digits of same place-values and retain it there itself. The final value will be derived by adding up all those numbers putting them in their respective places, i.e. adding them after multiplying by their respective place-values.

For example, let us consider the addition of two n-digit numbers A and B with base or radix r. In that case we can express these numbers as

$$A = a_n r^n + a_{n-1} r^{n-1} + \cdots + a_0 r^0,$$

and

$$B = b_n r^n + b_{n-1} r^{n-1} + \cdots + b_0 r^0 \tag{1}$$

The addition of these two numbers can be expressed as

$$A + B = (a_n + b_n) r^n + (a_{n-1} + b_{n-1}) r^{n-1} + \cdots + (a_0 + b_0) r^0 \tag{2}$$

Therefore, one can do the subsequent summations in any order. For a computer it is preferable to compute them parallelly. And the final sum will be calculated after suitable shifting operation.

This method works, since for any place, the value for $(a_n + b_n)$ can not exceed r; i.e. there cannot be any 'carry' in any places other than the most significant digit. And to ensure this condition, the number of addends must not exceed r. In other words, if S be the set of the addends, i.e.

$$S = \{A, B, \ldots\}, \tag{3}$$

Then, the cardinality of S, $|S| \leq r$.

However, there is no restriction over the number of bits n.

For example, in case of binary addition we should not take more than two numbers for the operation, but we can increase the number of bits as per our requirements.

QUANTUM CIRCUIT IMPLEMENTATION

The quantum representation of the two numbers can be written as

$$|A\rangle = |a_n a_{n-1} \dots a_1 a_0\rangle$$

And

$$|B\rangle = |b_n b_{n-1} \dots b_1 b_0\rangle \quad (4)$$

Here, the addition is done following eqn 2.

$$|A + B\rangle = |(a_{n+} b_n)\ (a_{n-1} + b_{n-1}) \dots (a_1 + b_1)\ (a_0 + b_0)\rangle \quad (5)$$

Following the above logic here we present a quantum circuit for the addition operation using Controlled-Not gates. There is no need to use carry in Lilavati – Bhashkaracharya Method, therefore only half adder (HA) is needed for n-bit addition. All the bit-wise summation operations are done parallelly in HA in the first step, in the next step a place-value wise shifting operation is done, and finally the last HA gives the concluding result.

Two bit quantum half adder circuit is shown in Figure1. Here HA represents the half adder circuit, which is made using standard procedure and shown along with the final circuit. The first two inputs (|1>) at the left, are the two addends and the last input (|0>) is the auxiliary input. On the right hand side, the last two outsputs are the Sum and Carry of the circuit respectively, and the value of the first wire is ignored. Two Controlled NOT (CNOT) gates are used to do the operation.

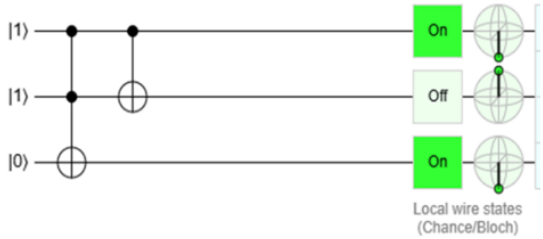

FIGURE 1. Quantum half adder circuit

The truth table of Figure 1 is given in table 1.

TABLE 1. Quantum half adder truth table

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

PROCEDURE

The schematic diagram of n-bit Lilavati – Bhashkaracharya Adder circuit is shown in Figure2.

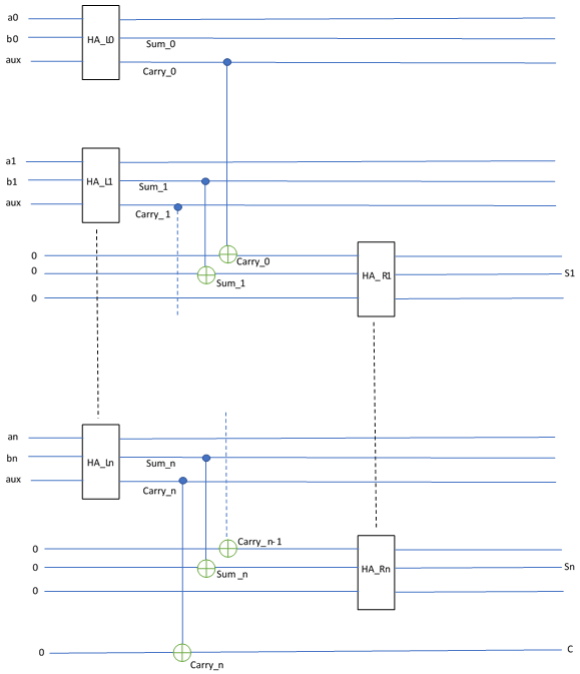

FIGURE 2. Schematic diagram of n-bit Lilavati – Bhashkaracharya Adder

The figure depicts the use of total 2n+1 number of HAs for n-bit addition, among which the left hand side HAs (HA_L0 – HA_Ln) are used to take the inputs and perform the bit-wise addition, while the right hand side HAs are used to generate the final result. In between these two sets, proper shifts operations were made in order to assign place-values to the bits – namely, the carry of one left HA is added to the sum of its next one using the corresponding right HA. The sum of the first HA_L0 and the carry of the last HA_Ln come out unchanged as least significant bit and most significant bit respectively. The other final bits are found from the sum port of right HAs.

Here we show an example of a two bit addition using this method in Figure3. To perform this operation we took the help of open platform software Quirk.

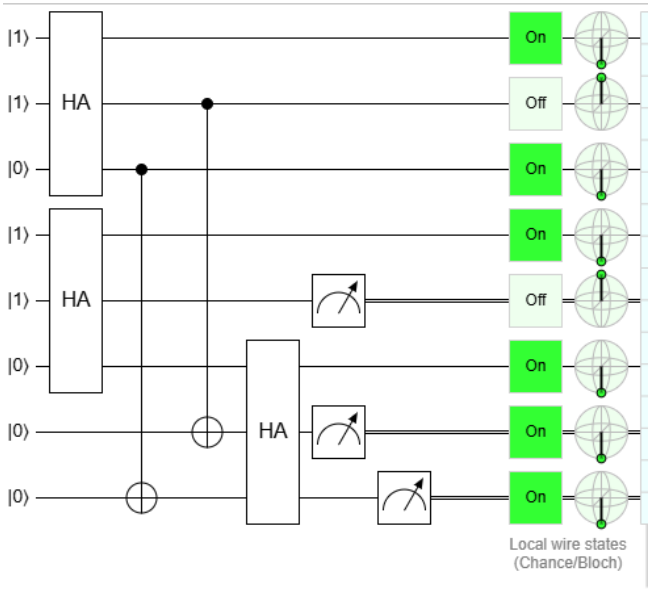

FIGURE 3. Two bit adder circuit using Lilavati principle

Two 2-bit binary numbers $|A\rangle = |a_1 a_0\rangle$ and $|B\rangle = |b_1 b_0\rangle$ are taken for addition. Here we need three half adders (HA) to perform this operation. Here HA0 adds a_0 and b_0 to generate Sum0 and Carry0 outputs. And HA1 adds a_1 and b_1 forming Sum1 and Carry1. These two operations are done simultaneously in the first unit of time. Now S0 from the HA0 will remain unchanged and that will produce the final LSB; whereas Sum1 from the HA1 and Carry0 from the HA0 are added after shifting the output of HA0 by one bit position to the left. This operation of one bit shifting corresponds to assigning place-value to the bits and this is done on the second unit of time. In the next and final stage these carry0 and sum1 are added using HA2 generating$|CS_1S_0\rangle$.
For example, here we have taken two binary numbers 11 and 11 (corresponding to 3 and 3 in decimal) for addition and received the output from terminals $|CS_1S_0\rangle$ as $|110\rangle$ (corresponding to decimal 6).

CONCLUSION

The Lilavati-Bhashkaracharya inspired quantum addition method introduces a novel approach to arithmetic in quantum computing. It drastically reduces circuit complexity, timing, and resource usage by removing carry propagation and using only half adders. This historical technique offers a highly efficient and parallelizable alternative to conventional quantum adders and underscores the timeless value of classical mathematical insights.

REFERENCES

1. Yasuhiro TAKAHASHI, "Quantum Arithmetic Circuits: A Survey" in IEICE TRANSACTIONS on Fundamentals, vol. E92-A, no. 5, pp. 1276-1283, May 2009, doi: 10.1587/transfun.E92.A.1276.
2. Wang, S., Li, X., Lee, W.J.B., Deb, S., Lim, E. and Chattopadhyay, A., 2025. A comprehensive study of quantum arithmetic circuits. Philosophical Transactions A, 383(2288), p.20230392.
3. Haener, T., Soeken, M., Roetteler, M. and Svore, K.M., 2018, August. Quantum circuits for floating-point arithmetic. In International conference on reversible computation (pp. 162-174). Cham: Springer International Publishing.
4. Muñoz-Coreas, E. and Thapliyal, H., 2019, July. Design of quantum circuits for cryptanalysis and image processing applications. In 2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) (pp. 360-365). IEEE.
5. Ghodsollahee, I., Davarzani, Z., Zomorodi, M., Pławiak, P., Houshmand, M. and Houshmand, M., 2021. Connectivity matrix model of quantum circuits and its application to distributed quantum circuit optimization. Quantum Information Processing, 20, pp.1-21.
6. Bhashkaracharya. (12th century). Lilavati.
7. Nielsen, M. A., & Chuang, I. L. (2010). Quantum Computation and Quantum Information. Cambridge University Press.
8. Vedral, V., Barenco, A., & Ekert, A. (1996). Quantum networks for elementary arithmetic operations. Physical Review A, 54(1), 147.
9. Shende, V. V., Bullock, S. S., & Markov, I. L. (2004). Synthesis of quantum-logic circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 25(6), 1000-1010.