Design of a Voltage Controlled Millimeter-Wave Oscillator for 5G/6G Applications in 180nm CMOS Technology

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***Abstract*—The paper presents the design of a voltage controlled mm-wave oscillator in 180nm CMOS technology. The oscillator provides a frequency of about 100GHz suitable for 5G/6G applications. The circuit is based on a fourth order LC network giving oscillation for IC realizable component values. Here we have extended the oscillator design by adding the tunability feature to it. This has been accomplished by using PMOS capacitors and changing the capacitance value by controlling the depletion region capacitance through the substrate terminal. The oscillator draws a power of 16.245mW from 1.8V supply and achieves a spot phase noise of -91.39dBc/Hz @1MHz offset. Such high oscillation frequency and tunability at higher technology node (low cost) has not been seen in the present literature.**

Keywords—180nm CMOS technology, 5G/6G applications, Millimeter-wave frequency, MOS capacitors, Oscillators, Phase noise

I. INTRODUCTION

The 4G network is almost saturated. The ever-increasing demand for higher data rates, ultra-low latency and ubiquitous connectivity in the wireless communication sector has pushed the RFIC design towards 5G/6G technologies. These operate in the mm-wave frequency band which lies between the microwave and infrared frequencies. Now 5G/6G transceivers invariably uses a voltage controlled oscillator (VCO) in the transmit and receive path and hence it is a critical component that must be designed. The designs are typically done in lower technology nodes as at these nodes, the cut-off frequency (f_T) is higher. But the associated fabrication cost is increased. 180nm CMOS technology is a very popular technology and in developing countries it is easily available. Hence, if 5G/6G oscillators can be designed in 180nm technology then the cost will be less and be easily marketable to the teeming masses. In this work we have designed a 100GHz mm-wave oscillator and added a tuning circuitry at this popular node.

[1] have designed a mm-wave oscillator at 27.5GHz where the oscillator is injection-locked by the 5th harmonic of a 5.5GHz reference. The implementation technology used is 65nm partially depleted SOI CMOS. Both the technology and oscillation frequency is lower than our work. [2] have designed a 77GHz VCO using a tunable inductor in 65nm single-poly 6-metal bulk CMOS technology. The technology node as well as the oscillation frequency is lower than ours. [3] have proposed a wideband mm-wave harmonic injection-locked oscillator in 130nm BiCMOS technology. The cascaded oscillator consists of a Class-F23 VCO (which is realized by a transformer-based resonant cavity) and a mm-wave injection-locked frequency tripler. The maximum fundamental frequency is 13.74GHz. Both the parameters are lower than ours. [4] have designed a wide tuning range low phase noise mm-wave CMOS VCO in 65nm CMOS technology. The architecture benefits from a switchable transformer-based LC tank which significantly improves the tuning range without compromising the phase noise performance. The maximum achievable frequency is 59.8GHz. As with the previously cited papers, [4] falls short to us in terms of technology node and oscillation frequency figures. [5] have proposed two 60GHz mm-wave VCOs (lower oscillation frequency than ours) in 28nm ultrathin body and buried oxide fully depleted silicon on insulator CMOS process (lower technology node than ours). The designs are for low noise performance.

We have designed a mm-wave oscillator which is based on a passive 4th order LC network. It has been analysed in [6]. The oscillator designed by [6] is at a frequency of 80GHz. We have extended the design to 100GHz at 180nm CMOS technology. We have added tuning circuitry to it which was not there in [6]. The tuning is accomplished by MOS capacitors in the variable capacitance portion of the C-V characteristic. The novelties of the design are as follows : higher oscillation frequency design at lower technology node and incorporation of tuning at that high frequency.

The rest of the paper is organized as follows. In Section II, the oscillator design is presented and analysed as well as the tuning circuitry. In Section III, the simulation results are provided while Section IV gives the conclusion.

II. VCO DESIGN AND ANALYSIS

The circuit diagram of the oscillator with ideal and non-ideal components are shown in Fig. 1 and Fig. 2 respectively.

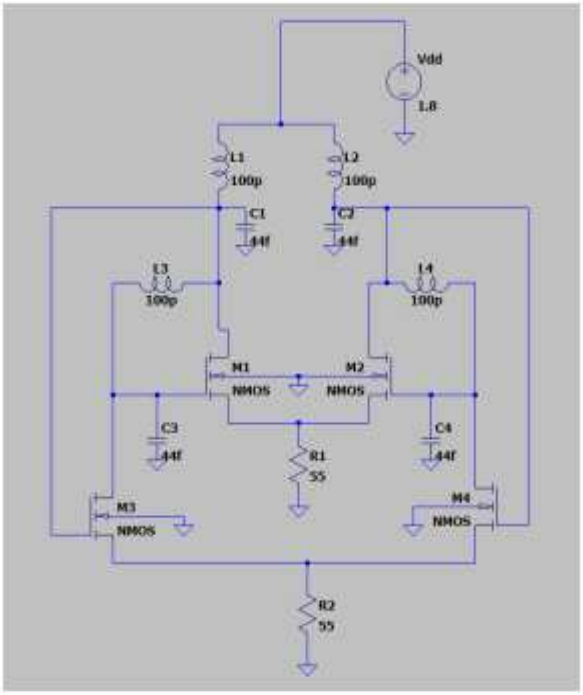

Fig. 1. Circuit with ideal components.

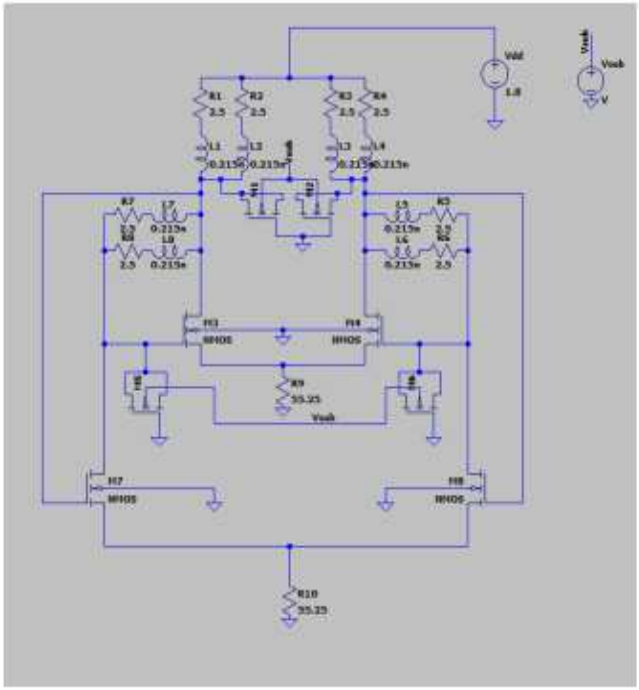

Fig. 2. Circuit with non-ideal components.

The circuit in Fig. 1 is based on a passive fourth-order LC network. The network [6] is shown in Fig. 3.

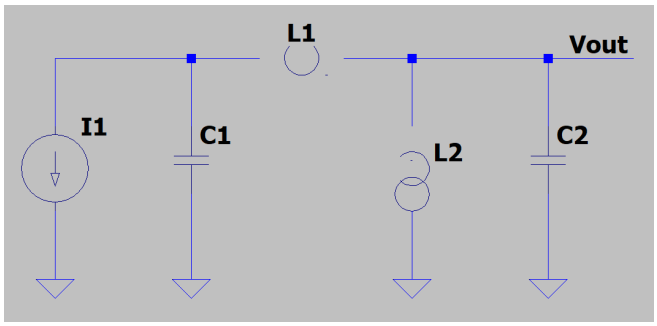

Fig. 3. Fourth-order passive LC network.

The transfer function is expressed as :

$$H(s) = \frac{-L_2 s}{L_1 L_2 C_1 C_2 s^4 + [(L_1 + L_2)C_1 + L_2 C_2]s^2 + 1} \quad (1)$$

When L_1=L_2=L and C_1=C_2=C, the transfer function exhibits two imaginary poles at :

$$\omega_{p2,p2'} = \pm j\sqrt{\frac{3+\sqrt{5}}{2LC}} \quad (2)$$

The magnitude of $\omega_{p2,p2'}$ is approximately 62% greater than the resonance frequency of second-order tanks, a critical advantage of the proposed technique. The inductors give loss which is compensated by the active devices. The minimum g_m required for oscillation is given by the following equation :

$$g_m = \frac{3\sqrt{5}+5}{2} \cdot \frac{1}{R} \quad (3)$$

In (3), R is the loss of the inductors at the oscillation frequency. In Fig. 2, the capacitors are made using PMOS capacitors. The inductors' values are too small to be realized in 180nm technology. So, two inductors in parallel are used to accomplish the task. The inductors are simulated with their equivalent series resistances giving a finite Q. Tail current sources are not used as their parasitics would load it at the oscillation frequency. Instead, resistors are used at the source-coupled points.

Frequency variation is done by tuning the PMOS capacitors. The process used is a n-well process so the PMOS capacitors have an explicit substrate connection. All the substrate terminals are shorted together to have one tuning line. Now, when the PMOS capacitors are in the depletion region of operation, if the substrate bias is varied, the depletion region thickness changes. This alters the depletion region capacitance and the total capacitance (which is the series combination of the oxide capacitance and the depletion region capacitance) changes, changing the oscillation frequency. The tuning is analog.

III. Results

The circuit has been designed in 180nm gpdk technology library. The simulator used is Cadence Virtuoso with 1.8V power supply. The maximum frequency of oscillation is 104.35GHz.

A snapshot of the oscillator waveform is shown in Fig. 4.

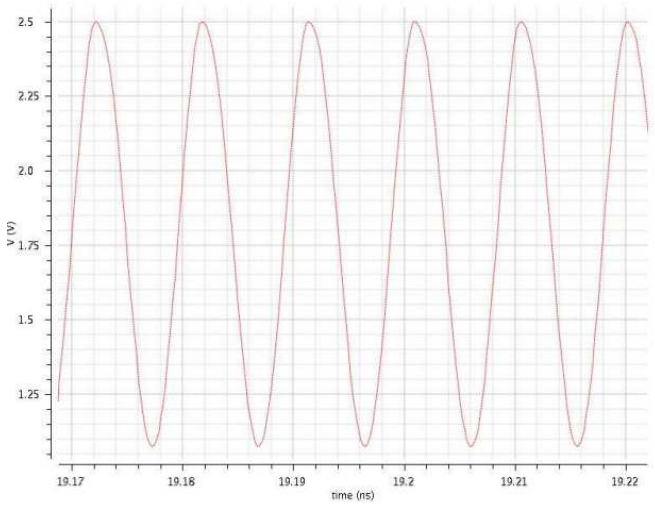

Fig. 4. Oscillator waveform.

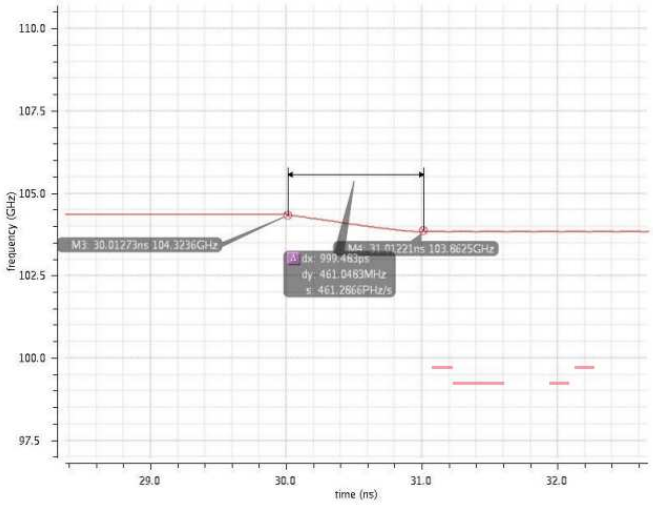

Fig. 5. Settling time plot.

The impact of process variation on the oscillation frequency is shown in Table I at T=300K and V_{sub}=1.8V.

TABLE I. PROCESS VARIATION VERSUS OSCILLATION FREQUENCY

Process corner	Oscillation frequency (GHz)
Typical	104.35
Slow	105.65
Fast	103.9

The temperature variation of the oscillator is shown in Table II.

TABLE II. TEMPERATURE VARIATION VERSUS OSCILLATION FREQUENCY

Temperature (K)	Typical	Slow	Fast
273	104.54GHz	105.85GHz	104.07GHz
343	104.07GHz	105.35GHz	103.61GHz

The effect of supply variation on the oscillator is shown in Table III at T=300K and V_{sub}=1.8V.

TABLE III. SUPPLY VOLTAGE VARIATION VERSUS OSCILLATION FREQUENCY

Supply voltage (V)	Oscillation frequency (GHz)
1.62	104.05
1.70	104.18
1.80	104.35
1.90	104.34
1.98	104.23

The power consumption is 16.245mW.

The settling time (time taken to change from 104.32GHz to 103.86GHz) is 1ns. The settling time plot is shown in Fig. 5.

The phase noise plot of the oscillator is shown in Fig. 6.

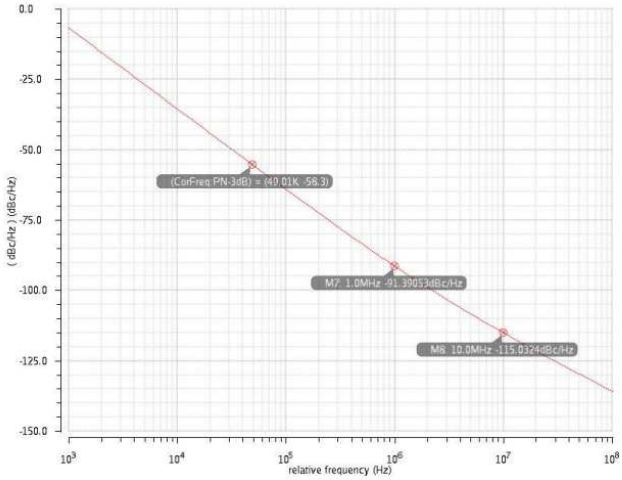

Fig. 6. Phase noise plot of the oscillator.

The oscillator exhibits a phase noise of -91.39dBc/Hz @1MHz offset and -115.03dBc/Hz @10MHz offset. Table IV shows the variation of frequency as the substrate voltage is varied.

TABLE IV. FREQUENCY VARIATION WITH SUBSTRATE BIAS CHANGE

Substrate voltage (V)	Oscillation frequency (GHz)
1.55	104.05
1.60	104.07
1.65	104.11
1.70	104.18
1.75	104.26
1.80	104.35

IV. CONCLUSION

In this paper, the design of a 100GHz mm-wave oscillator in 180nm CMOS technology has been presented. The oscillator can be used in 5G/6G applications. Tunability has

been incorporated by changing the substrate bias voltage of PMOS capacitors. Such high frequency operation in higher technology node with options for tuning has not been seen previously. It provides a solution for designing low-cost mm-wave radios especially in developing countries. Future work is to integrate a phase locked loop with it and realize the circuit in silicon.

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