

An Ultra-Low Power Low Phase Noise Pseudoresistive Astable Multivibrator for MICS Band Wireless Sensor Node Applications

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Abstract— The paper presents the design of an ultra-low power pseudoresistive astable multivibrator for Medical Implant Communications Service (MICS) band applications. Instead of tail current source, we have used a MOSFET operating in deep triode region (acting as pseudoresistor) which reduces the $1/f^3$ noise corner of the phase noise spectrum. Complementary MOSFETs have been used as switches for linearization of its output resistance which reduces the phase noise further. A resistor based tuning circuit provides bias to the pseudoresistor which can be used for changing the frequency. The outputs are pseudodifferential (accomplished by two cross-coupled low strength CMOS inverters) providing rejection to common-mode noise. The entire circuit has been designed and simulated in Cadence Virtuoso using gpd180 nm technology library and draws a current of $150\mu\text{A}$ from 1.8V power supply while achieving a phase noise of -100dBc/Hz @ 1 MHz offset. Such low phase noise performance at this ultra-low power has not been seen in other MICS band oscillators so far.

Keywords—Astable multivibrator, Medical Implant Communications Service (MICS) band, Phase noise, Pseudodifferential, Pseudoresistive, Ultra-low power

I. INTRODUCTION

Wireless sensor nodes (WSNs) consists of sensors and data acquisition circuitry, digital signal processing circuitry and a radio front-end. Of the three subsystems the radio section is the most power hungry and hence its power minimization is crucial. The radio front-end invariably uses an oscillator in the transmit/receive path. In this paper, we have designed an oscillator which not only consumes ultra-low power but also provides good phase noise performance. We have considered the Medical Implant Communications Service (MICS) band which caters to implanted biomedical telemetry in the $402\text{--}405\text{MHz}$ frequency range. Details about it can be found in [1]. For MICS band operation, the oscillator must have no external components; occupy low die area; must have fast start-up; be easily tunable; consume ultra low power and preferably have good phase noise performance. All these point to the use of a ring based topology. In this work, we have designed a CMOS based astable multivibrator whose frequency equation is similar to a one-stage ring oscillator and have added some novel features.

The first MICS band transceiver was designed by Zarlink Semiconductor Inc. and has been reported in [2]. The design consumed a high current of 5.5mA . A ‘super-low power’ receiver was reported in [3] where the total synthesizer power consumption was $370\mu\text{W}$. A LC VCO was used for RF frequency generation with passive polyphase filter for quadrature phase generation. The inductor values were 25nH which consumed huge chip area. A pioneering work in the MICS band was reported in [4] where a differential Colpitts oscillator was used in the transmit path. Although it achieved good phase noise performance the oscillator bias current was $450\mu\text{A}$ which was quite high. In [5] an injection locking based transmitter architecture has been designed where a low frequency carrier has been injection locked to a reference frequency and then was multiplied to the desired RF frequency. The oscillator current consumption was low ($90\mu\text{A}$). However, the design was limited to single channel operation. Also, higher data transmission was not feasible due to the limit on the amount of reference crystal frequency pulling. In [6-7], a self-calibrating PLL with ring voltage controlled oscillator (VCO) architecture has been used for data transmission, the power consumption of which was $800\mu\text{W}$. In [8], RF front-end for image transmission in MICS band has been designed. The modulation scheme used was GFSK (Gaussian frequency shift keying). A mixed loop modulation scheme has been followed but power consumed was 12.7mW . In [9], UWB (ultra wide band) transmitter architecture has been proposed that used a PN sequence followed by a pulse-shaper and differentiator structure. The work achieved power consumption of $300\mu\text{W}$ but assumed a complex base-station receiver. In [10], BPSK (binary phase shift keying) together with injection locked oscillator has been used as the Tx architecture. The work had a power consumption figure of 1.18mW .

In this work, we have used an astable multivibrator whose basic structure has been reported in [11]. Instead of a pass gate switch we have used a transmission gate switch whose resistance is more linear and hence improves phase noise performance. Instead of tail current source which injects $1/f$ noise we have used a pseudoresistor thereby improving the $1/f^3$ noise corner. Further low strength CMOS inverters at the output in a latch based configuration make the final output

pseudo-differential improving common mode noise rejection performance. The design achieves a current consumption of $150\mu\text{A}$ from 1.8V power supply in 180nm CMOS process and has a phase noise performance of -100dBc/Hz @ 1MHz offset. It addresses the shortcomings of the designs charted in the literature survey.

The rest of the paper is organized as follows : In Section II, the design of the oscillator is presented. In Section III, the results are provided, while Section IV gives the conclusion.

II. OSCILLATOR DESIGN

The oscillator circuit is depicted in Fig. 1 with the tuning circuitry in Fig. 2.

The oscillator circuit in its basic form (as shown in Fig. 1) consists of two switches through which a capacitance charges and discharges. The capacitor output is connected to a non-inverting Schmitt Trigger whose levels determine the triggering points. Once the upper level is reached, the pull down switch is ON and the capacitance discharges. The

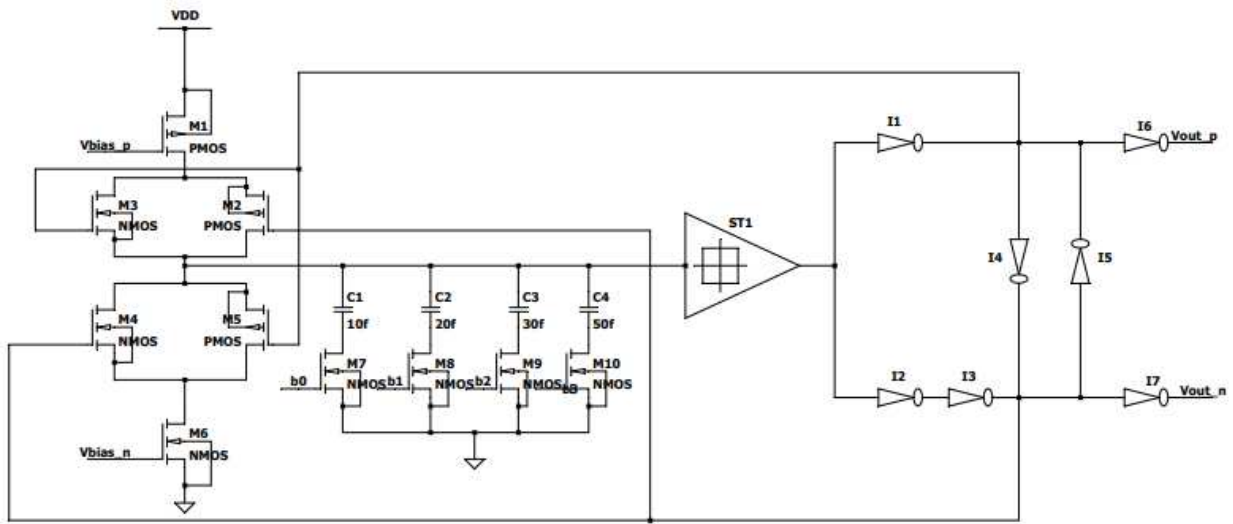


Fig. 1. Oscillator circuit diagram.

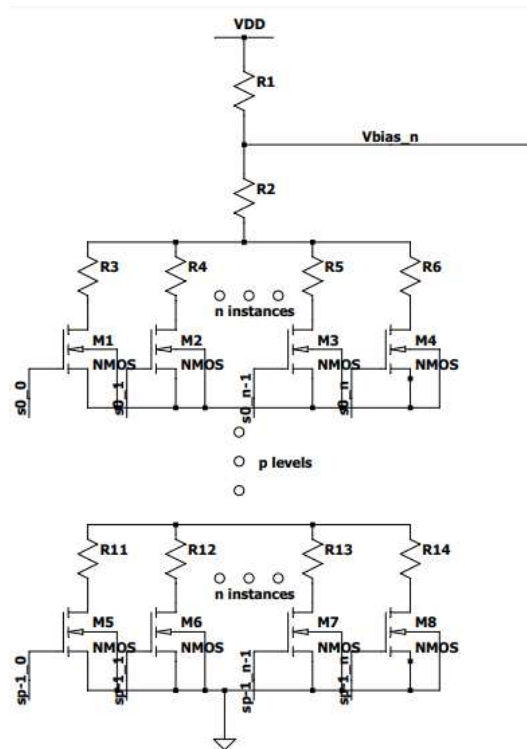


Fig. 2. Tuning circuit (NMOS section only).

capacitor voltage decreases and when it reaches the lower level, the pull up switch is turned ON and the capacitance charges. In this way, the capacitance voltage oscillates between two voltage levels and at the output of Schmitt Trigger we get a square wave.

Now in the pull up and pull down switches, we have added a complementary device so that as the capacitor voltage changes, the equivalent resistance remains more or less constant improving linearity and hence improving phase noise performance. The concept is akin to the use of a transmission gate switch instead of a pass gate switch. In contrast to the structure in [11] where the switch opens a current source/sink for charging/discharging, we have used a MOS in deep triode region acting as a pseudoresistor (through which the load capacitance charges/discharges). In a pseudoresistor the g_m is very low which improves the $1/f$ noise corner and hence the $1/f^3$ corner of the phase noise spectrum. The load capacitance is a switchable capacitance to account for process corner effects. Now, WSNs are battery powered devices and after prolonged use, the battery voltage may sag so a voltage regulator is essential to keep the supply voltage constant and power the analog/RF blocks. We have assumed that supply voltage is constant at 1.8V by means of a voltage regulator. Temperature variations are minimal as human body is an excellent temperature regulator [4]. The output of the non-inverting Schmitt Trigger is made complementary by inverters I_1 , I_2 and I_3 in Fig. 1. The delay of I_2 and I_3 is half of I_1 . Then two inverters (I_4 and I_5) in a latch configuration, whose strength is $1/4^{\text{th}}$ that of the driving inverters, make the output pseudodifferential. Then two inverters (I_6 and I_7) buffer the output before interfacing with another block.

The tuning circuitry (in Fig. 2) is basically a resistor divider. There are two fixed resistances which are big and the small resistances are switched. There are 'p' levels and in each level, there are 'n' switchable resistances. As we go from one level to the next, the resistance values are halved. In each level one resistance is ON. The PMOS tuning circuit is complementary to the NMOS tuning circuit.

III. RESULTS

The circuits have been designed in gpdk 180nm technology library using Cadence Virtuoso. The supply voltage is 1.8V. and the average current drawn from supply at 400 MHz is $150\mu\text{A}$. The picture of the oscillating waveform is shown in Fig. 3. The phase noise plot is shown in Fig. 4. From Fig. 4, it is seen that the phase noise is -100dBc/Hz @1MHz offset. The settling time plot is shown in Fig. 5. From it, we find that the oscillator takes 555.02ns to jump from 409.64MHz to 410.26MHz. The differential mismatch-rising and falling are shown in Fig. 6 and 7 respectively. From Fig. 6 and 7, we see that the mismatch is very small. The change in frequency by varying the switch resistance of the NMOS tuning network is depicted in Table I.

IV. CONCLUSION

In this paper, the design of a novel astable multivibrator based oscillator has been presented. The oscillator consumes ultra-low power and low area while providing good phase noise performance. It can easily be used in MICS band applications saving battery life and providing multi-channel operation – a feature not seen before in the present literature. Future work is to integrate a frequency synthesizer with it and realize the structure in silicon.

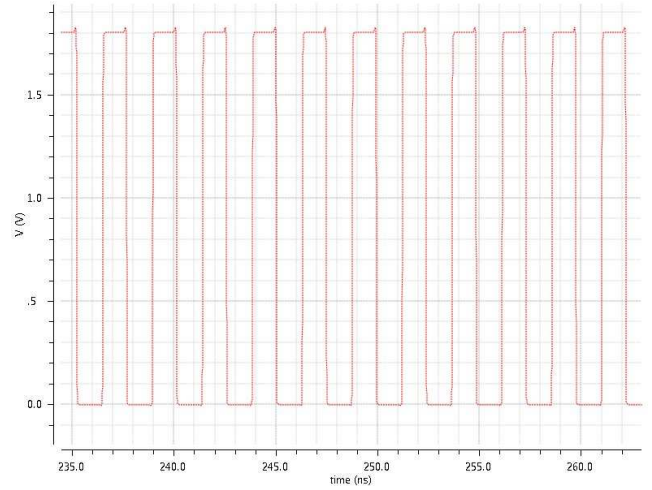


Fig. 3. Oscillating waveform plot.

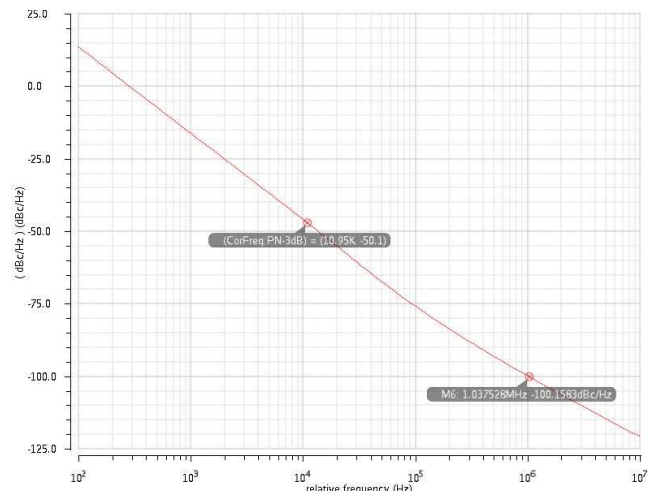


Fig. 4. Phase noise plot of the oscillator.

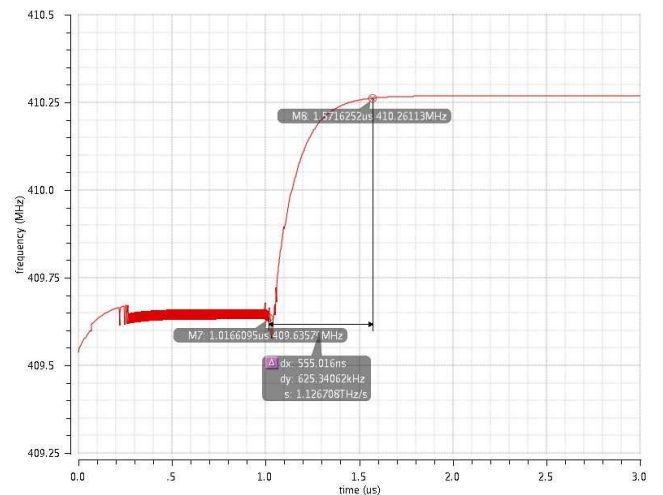


Fig. 5. Oscillator settling time plot.

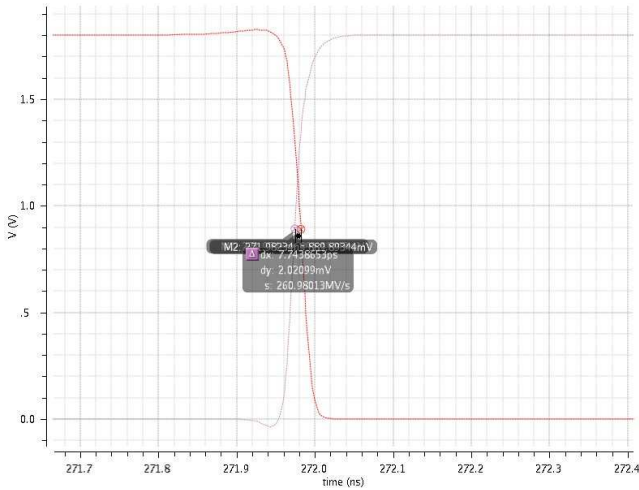


Fig. 6. Differential mismatch – rising.

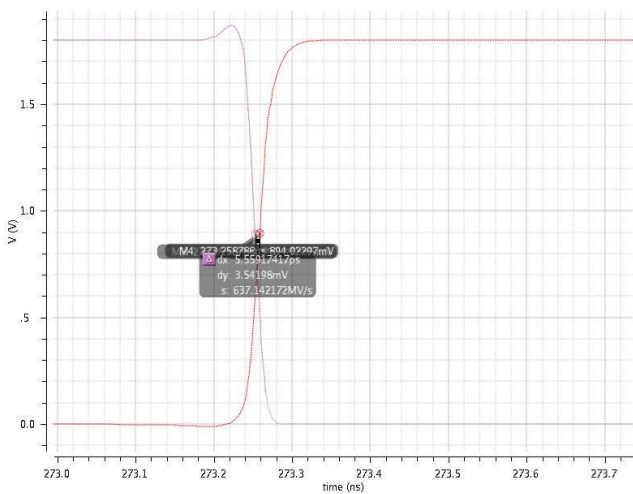


Fig. 7. Differential mismatch – falling.

TABLE I. NMOS SWITCH RESISTANCE VERSUS OSCILLATION FREQUENCY

NMOS switch resistance (K Ω)	Output frequency (MHz)
5.4	406.9
5.8	407.3
6.2	407.7
6.6	408.1
7.0	408.5
9.8	411.0

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