Design and FPGA Implementation of an Efficient Squarer Circuit Using Reversible Logic

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***Abstract*— This paper presents the design and FPGA implementation of an efficient 4x4 squarer circuit using reversible logic. The proposed architecture is developed using the hardware description language Verilog and synthesized with Xilinx Vivado and Xilinx ISE 14.7 tools. The FPGA implementation of proposed design has been done on Artix 7 (Nexys A7). The main improvements in this work include a significant reduction in garbage output, quantum cost, and total reversible logic implementation cost (TRLIC) compared to existing designs. Notably, the proposed architecture achieves quantum cost and TRLIC reductions of 84.34% and 82.10%, respectively. The circuit also demonstrates a remarkably low delay of 1.076 ns, making it suitable for high-speed applications.**

Keywords*— *Reversible logic, Squarer, Quantum Cost, Verilog, FPGA

I. Introduction

In the dynamic landscape of digital systems, two paramount objectives stand out: minimizing delay and reducing quantum cost. Delay, the interval between an input signal and the system's response, holds the key to unlocking speed and responsiveness in digital operations. Even marginal reductions in delay can yield substantial performance enhancements, enabling faster data processing and heightened real-time responsiveness. Similarly, the reduction of quantum cost is foundational in digital system design. Quantum cost represents the computational resources necessary for executing logic operations, encompassing gate count and complexity. By minimizing quantum cost, we not only optimize resource utilization but also pave the way for lower power consumption and improved scalability of digital circuits. Essentially, cutting quantum cost enables the creation of compact, energy-efficient designs endowed with heightened computational prowess.

Traditional logic gates—those trusty stalwarts like AND, OR, NOT, and XOR—bear inherent limitations in fulfilling these objectives. While they form the bedrock of digital circuitry, their association with significant delay and high quantum cost poses challenges in the face of escalating system demands. As digital systems evolve in complexity and sophistication, the constraints of traditional logic gates become more conspicuous, impeding the realization of high-performance and energy-efficient solutions. Furthermore, the specter of energy dissipation looms large over traditional logic gates, complicating the already intricate task of power management in digital systems. The perpetual generation of heat due to energy loss not only jeopardizes the reliability and durability of electronic components but also imposes constraints on system scalability and operational expenses. Hence, the pursuit of low-power solutions emerges as a critical imperative, offering a pathway to address these challenges and fortify the sustainability of digital systems.

II. Reversible Logic Gates

Reversible logic gates are based on injective functions, where every input function give a unique output. There is always a one-to-one mapping between the inputs and outputs i.e., Both inputs and outputs have an equal quantity. Gate count (N), constant inputs (CI) / ancilla inputs, garbage outputs (GO) and quantum cost (QC) are few essential elements should be considered during the constructing of reversible logic gates.

Gate count - The total number of reversible logic gates are required while designing the circuit.

Constant inputs / Ancilla inputs- The number of constant inputs either 0 or 1 are used to implement the logical function.

Garbage outputs- it refers to the outputs that are generated as a result but not a desired output during the designing of logical function using reversible gates. Minimum

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number of garbage outputs is more effective in implementation of logical function using reversible gates.

Quantum cost- in reversible quantum computing one of the most important parameters is Quantum cost which refers to the cost of the circuit in terms of the cost of a primitive gate. The calculation process is the number of primitive reversible logic gates (1*1 or 2*2) needed to recognize the circuit.

III. Reversible Logic Gates Used in Proposed Work

A. Peres Gate (PG)

Peres Gate is a reversible gate with 3 inputs (U, V, W) and same number of outputs (M, N, O) where M=U, N=U⊕V, O=UV⊕W. 4 is the quantum cost of Peres gate.

M=U

N=U ⊕V

O=UV ⊕W

B. Hybrid New Gate (HNG)

Hybrid New Gate (HNG) is a universal reversible gate with 4 inputs (U, V, W, X) and same number of outputs (M, N, O, P) where M=U, N=V, O=U ⊕V ⊕W, P= (U ⊕V) W ⊕UV⊕X. Quantum cost of Hybrid New Gate is 6.

M=U

N=V

O=U ⊕V ⊕W

P= (U ⊕V) W⊕UV ⊕X

IV. Proposed 4x4 Squarer Circuit

Squaring is basically a multiplication of two same numbers. This section of the paper shows quantum circuit for squaring of an operand. Fig:1 represents the partial product generation for square operation of a 4-bit operand. In middle section of the Fig:1 shows the partial product array in which the combining of some products terms generate using the similar equation $a_i \bullet a_j + a_i \bullet a_j = 2 \bullet a_i \bullet a_j$. Rectangular boxes present possible equivalence form the generated product terms. Following the application of the equation to these product terms, product phrases gain two times more weight as shown in the following column. Full adder and Half adder are used for the summation part of the circuit. Full adder is a combinational circuit use for adding three binary digits and result in terms of sum and carry where Half adder is used for addition of 2 binary digits. The arrows represent the moving of combined product phrases left by one position. Lastly, the reduced partial products are displayed in the final column of Fig:1.

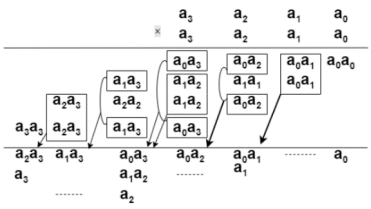

Fig. 1. Partial product generation [2]

The full squarer circuit is represented in Fig:4 where AND gate is used for partial product generation. In next step Full adder and Half adder are used for reducing the partial product terms. In Fig:4 a_0, a_1, a_2, a_3 are the input digits of a 4-bit binary number and Y_0, Y_1, Y_2, Y_3, Y_4, Y_5, Y_6, Y_7 are final output of the squarer circuit which is square of the input number.

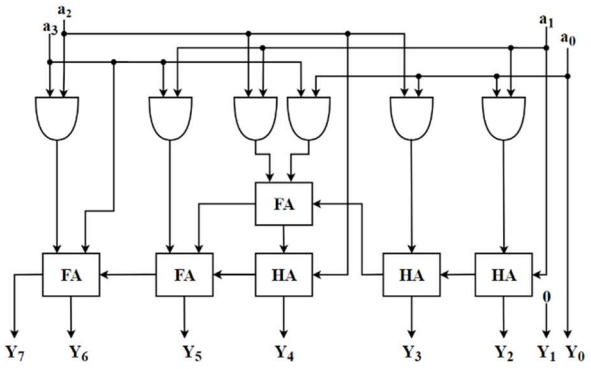

Fig. 2. Squarer circuit

A. Partial Product Generation Using Reversible Logic

The first step for performing square operation is to generate the product terms using reversible logic. For generating the partial product terms and reducing the terms Peres gates are used. For implementing AND operation, the input W of the Peres gate is fixed at zero which is an ancilla input (zero is constant). Their connections to one another are made in series. Peres gate is used because quantum cost of this gate is 4 which is less than Toffoli gate. In Fig:3 a_0, a_1, a_2,a_3 are the inputs and m_0, m_1, m_2, m_3, m_4, m_5 required products terms for summation. Some output of each Peres gate relates to another Peres gate or to the summation part.

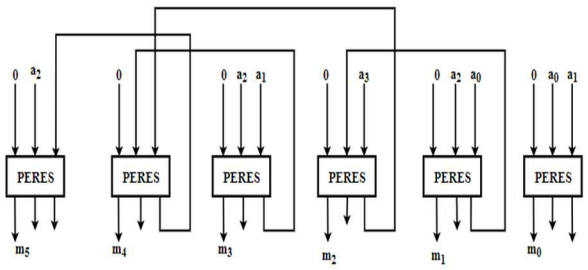

Fig. 3. Block diagram of partial product generation

B. Summation of Reduced Partial Product Terms

The final reduced products in 4-bit squarer unit are generated by carry save method in summation stage. For this architecture the reversible full adder and half adder blocks are required. HNG gates are used to design a full adder where input X=0 as displayed in Fig:5. similarly, for half adder Peres gates are used by keeping input W=0 as displayed in Fig:4. Y_2, Y_3, Y_4, Y_5, Y_6 are few output digits of the squarer circuit present in the Fig:3. The summation circuit for the full squarer circuit is illustrated in fig.4.

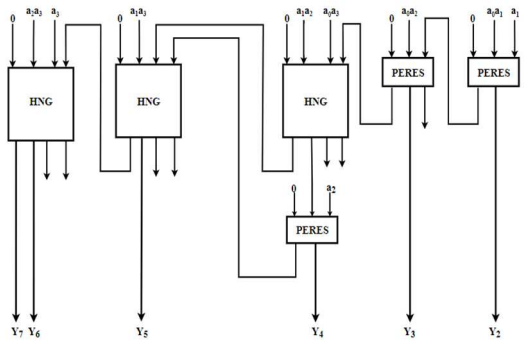

Fig. 4. Summation circuit block diagram for 4*4 square unit

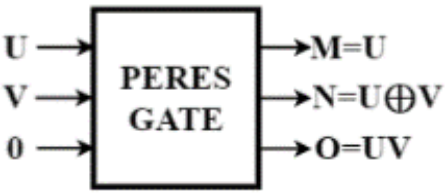

Fig. 5. Half adder using Peres gate

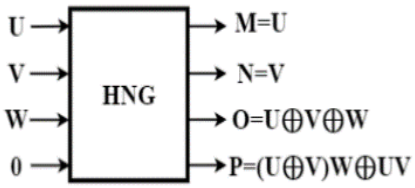

Fig. 6. Full adder using HNG gate

V. SIMULATION AND RESULT

The proposed reversible squarer architecture is validated by simulation. Fig.10 shows the RTL of proposed architecture. For checking proper functioning of the circuit, 3 random inputs have been taken, which has been organized in a tabular form in table.1. Fig.7, fig.8, fig.9 represents the simulation results of 3 different test cases.

TABLE I. TEST CASE RESULT IN SIMULATION

TEST CASE	INPUT	OUTPUT
1	0111	00110001
2	1010	01100100
3	1101	10101001

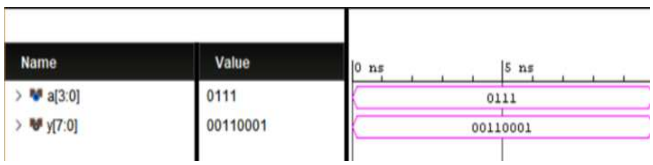

Fig. 7. Simulated output of test case 1

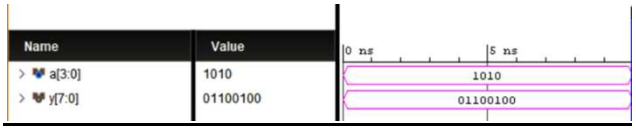

Fig. 8. Simulated output of test case 2

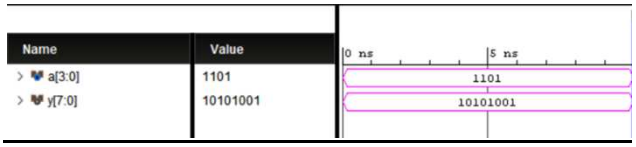

Fig. 9. Simulated output of test case 3

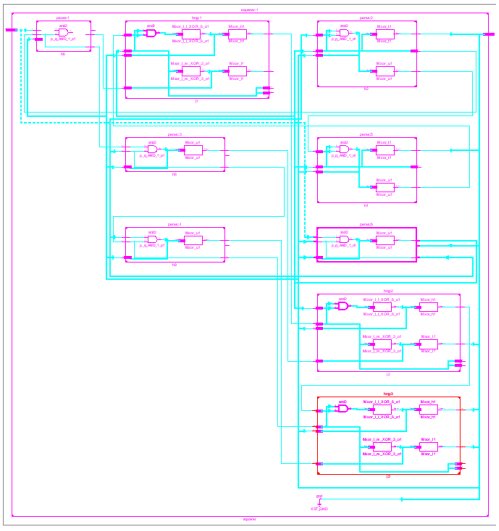

Fig. 10. RTL view if the circuit

The delay of the proposed design using NEXYS A7 - xc7a100tcsg324-1 (Artix-7 series) is obtained 1.076 ns and the device static power of the proposed design is obtained 0.136 W.

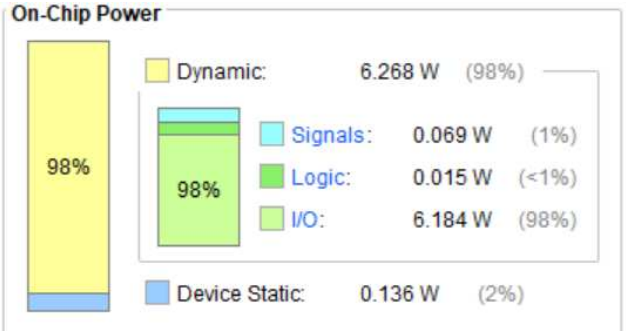

Fig. 11. On-Chip power during FPGA implementation

In table 2. It is visible that just 12 reversible gates were used in the proposed design of the squarer. The circuit contains 13 garbage outputs, 13 ancilla inputs,

and quantum cost of 54. Table displays the comparative analysis and improvement with the existing design.

TABLE II. COMPARISON WITH EXISTING DESIGN

Parameter	Gate Count	Ancilla Input	Garbage Output	Quantum Cost	% of improvement	TRLIC	% of improvement
Proposed Design	12	13	13	54		92	
Ref [2]	12	13	09	60	10%	94	2.12 %
Ref [5]	32	36	28	196	72.44 %	292	68.49 %
Ref [6]	28	28	28	196	72.44 %	280	67.14 %
Ref [7]	52	28	52	290	81.38 %	422	78.19 %
Ref [8]	53	58	58	345	84.34 %	514	82.10 %
Ref [9]	80	76	50	298	81.87 %	504	81.74 %

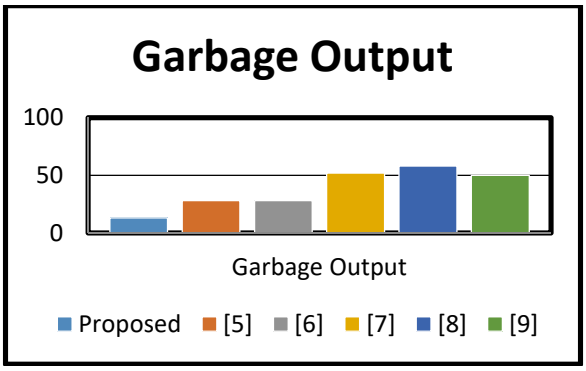

Fig. 12. Comparison of garbage output

VI. FPGA IMPLEMENTATION

FPGA Implementation of the proposed design has been done on NEXYS 7 (Artix 7 series) Fpga. Figure 13 shows the fpga implementation of test case 1 where each led represents one bit of output. For the implementation switches pin of J15, L16, M13 and R15 are used for input, R15 represents MSB bits of input, and from leds H17 represents the MSB of outputs. Blinking led results in binary 1 and turned off light results in binary 0. It can be observed that the simulated output and the FPGA functioning outputs are similar.

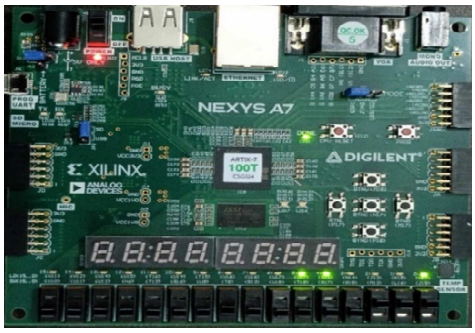

Fig. 13. FPGA implementation of test case 1

VII. CONCLUSION

This paper presents a high-speed, efficient squarer circuit design utilizing reversible logic, specifically implemented on an FPGA. The proposed architecture, realized using Verilog and synthesized with Xilinx Vivado and ISE 14.7 tools, demonstrates substantial improvements over traditional designs. Targeting the Artix-7 FPGA, the design achieves significant reductions in delay, garbage output, quantum cost, and TRLIC. Notably, the proposed architecture reduces quantum cost by 84.34% and TRLIC by 82.10%, while maintaining a remarkably low delay of 1.076 ns.

These advancements highlight the potential of reversible logic in creating more efficient and high-performance digital circuits. By addressing key challenges in power dissipation and resource optimization, the proposed design offers a promising approach for future digital system development. Future work will explore further optimizations and broader applications of this design methodology to various computational domains, aiming to continue the trend towards more efficient and powerful digital solutions.

REFERENCES

[1] Halder, Saurabh & Saha, Mihir & Malvika, Malvika & Talukdar, Jagritee & Mummaneni, Kavicharan. (2023). Design and Implementation of an Optimized High-Speed Vedic-Based Squarer Circuit Using Reversible Logic Gates. 10.1007/978-981-99-4495-8_24.

[2] Patil, S. S., Patil, M., & Appa, V. (2018). FPGA IMPLEMENTATION OF 4-BIT AND 8-BIT SQUARE CIRCUIT USING REVERSIBLE LOGIC (5th ed., pp. 86-90). International Journal of Current Engineering And Scientific Research (IJCESR).

[3] MANTUR, S., M V, C. M., KURIAN, M. Z., & GURUPRASAD, H. S. (2013). Design of 4x4 Reversible Square Quantum Circuitry. *International Journal of Emerging Technology in Computer Science & Electronics (IJETCSE)*, *14*(2).

[4] H. V. Jayashree, H. Thapliyal and V. K. Agrawal, "Design of Dedicated Reversible Quantum Circuitry for Square Computation," *2014 27th International Conference on VLSI Design and 2014 13th International Conference on Embedded Systems*, Mumbai, India, 2014, pp. 551-556, doi: 10.1109/VLSID.2014.102.

[5] Peres, A. (1985). Reversible logic and quantum computers. *Phys. Rev. A*, *32*(6), 3266-. https://doi.org/10.1103/PhysRevA.32.3266

[6] T.D.Nguyen, and R.Van Meter, "A Space Efficient Design for Reversible Floating Point Adder in Quantum Computing", arXiv preprint arXiv: 1306.3760,2013.

[7] S. Kotiyal, H. Thapliyal and N. Ranganathan, "Circuit for Reversible Quantum Multiplier Based on Binary Tree Optimizing Ancilla and Garbage Bits," 2014 27th International Conference on VLSI Design and 2014 13th International Conference on Embedded Systems, Mumbai, India, 2014, pp. 545-550, doi: 10.1109/VLSID.2014.101.

[8] Thapliyal, Himanshu & Srinivas, M.B. (2006). Novel Reversible Multiplier Architecture Using Reversible TSG Gate. IEEE International Conference on Computer Systems and Applications, 2006. 2006. 100- 103. 10.1109/AICCSA.2006.205074.

[9] Banerjee, A. and Pathak, A., 2009. An analysis of reversible multiplier circuits. arXiv preprint arXiv:0907.3357.

[10] R. Landauer, "Irreversibility and Heat Generation in the Computing Process," in *IBM Journal of Research and Development*, vol. 5, no. 3, pp. 183-191, July 1961, doi: 10.1147/rd.53.0183.

[11] C. H. Bennett, "Logical Reversibility of Computation," in *IBM Journal of Research and Development*, vol. 17, no. 6, pp. 525-532, Nov. 1973, doi: 10.1147/rd.176.0525.

[12] Vedral, Vlatko et al. "Quantum networks for elementary arithmetic operations." *Physical review. A, Atomic, molecular, and optical physics* 54 1 (1995): 147-153.

[13] Takahashi, Y. (2009). Quantum Arithmetic Circuits: A Survey. *IEICE Trans. Fundam. Electron. Commun. Comput. Sci., 92-A*, 1276-1283.

[14] S. F. Obermann and M. J. Flynn, "Division algorithms and implementations," in *IEEE Transactions on Computers*, vol. 46, no. 8, pp. 833-854, Aug. 1997, doi: 10.1109/12.609274.

[15] M. Nachtigal, H. Thapliyal and N. Ranganathan, "Design of a reversible single precision floating point multiplier based on operand decomposition," *10th IEEE International Conference on Nanotechnology*, Ilsan, Korea (South), 2010, pp. 233-237, doi: 10.1109/NANO.2010.5697746.

[16] W. N. N. Hung, Xiaoyu Song, Guowu Yang, Jin Yang and M. Perkowski, "Optimal synthesis of multiple output Boolean functions using a set of quantum gates by symbolic reachability analysis," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 9, pp. 1652-1663, Sept. 2006, doi: 10.1109/TCAD.2005.858352.

[17] Naderpour, Fateme &Vafaei, Abbas. (2009). Reversible multipliers: Decreasing the depth of the circuit. 306 - 310. 10.1109/ICECE.2008.4769222.

[18] Islam, M., Rahman, M., Begum, Z., & Hafiz, M. (2009). Reversible logic and quantum computers. *Information Technology Journal*, *8*(2), 208-213. https://doi.org/10.3923/itj.2009.208.213