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# High Frequency Control Logic Design for Asymmetrical Input CHB Inverters

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***Abstract*—This work reports twelve switches cascaded H bridge (CHB) multilevel inverters (MLI) for asymmetrical input sources and high frequency control strategies. The proposed inverter consists of only twelve switches and is able to generate up to 27 level through asymmetrical switching as well as high frequency-based multi-carrier pulse width modulation (MCPWM) techniques. All the expressions for the switch logic to generate 7 level to 27 level are provided in the methodology sections and a few simulation results are plotted for the realization of the control techniques. As the proposed inverter is capable to generate higher levels with the suggested control strategy, the topology will automatically be claimed as a reduced switch and component count structure. The total harmonic distortion (THD) is improved in the output as the number of levels is getting increases.**

***Keywords—Twelve Switch CHB, MCPWM, Asymmetrical Input, THD.***

## I. INTRODUCTION

Conventional multilevel inverters (MLI) are classified as neutral point clamped (NPC), flying capacitor or capacitor clamped (FCC), and cascaded H bridge (CHB) inverters. MLI system has become more promising because of high power quality, reduced filter size, scalability, and controllability, and in the field of renewable power generation or electric vehicle applications [1]. The NPC and FCC aggregate huge switches and component counts with the increase in number of levels. On the other hand, CHB reduces the switches and component count compared to the previous structures with the generation of a same number of levels [2]. Besides, CHB has the property of high modularity and switching state redundancies including the capability of additive and subtractive polarity of switching. For this reason, till now, CHB is the most used traditional MLI topology in industrial and commercial applications [2].

Modulation and control strategies for MLI can be either high frequency based or low frequency based. Low frequency control generates high magnitude lower order harmonics whereas high frequency control produces reduced magnitude higher order harmonics. MCPWM techniques can be used for both level-shifted and phase-shifted PWM strategies. Here, level-shifted PWM is proposed as it produces comparatively less THD. Level-shifted PWM techniques are phase disposition (PD), phase opposition disposition (POD), alternate phase opposition disposition (APOD), and variable frequency PWM (VFPWM) [3]. Generation of switch logic expressions for asymmetrical switching is a tedious job for the high frequency control. For this reason, high frequency control is selected to generate the different levels by using CHB.

In this work, high frequency PD technique is used to describe the MCPWM control for the generation of different levels by using 12 switches CHB inverter. The input logic expressions for all the possible levels (7 to 27) are shown to realize the high frequency control. The output voltages and currents are shown for the designed levels.

## II. CHB TOPOLOGY

Fig. 1 shows the proposed 12 switches CHB topology. It has twelve switches ($T_1$ to $T_{12}$), and three DC input sources, i.e., the total component count is fifteen. The input voltages are $V_1$, $V_2$, and $V_3$ can be combined either symmetrically or asymmetrically to produce a maximum 27 levels by this topology. How the DC input sources are given to generate the required levels are listed in Table I.

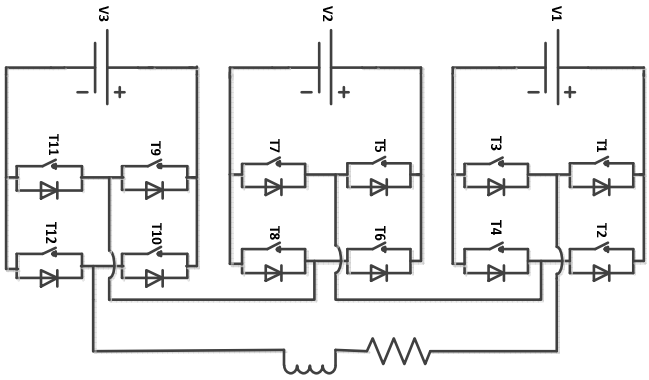



Fig. 1. Proposed CHB inverter

TABLE I. DC INPUT SOURCES & OUTPUT VOLTAGE LEVELS

| Input Source Combination | Output Voltage Level |
|---|---|
| $V_1$=V, $V_2$=V, $V_3$=V | 7 Level |
| $V_1$=V, $V_2$=V, $V_3$=2V | 9 Level |
| $V_1$=V, $V_2$=2V, $V_3$=2V | 11 Level |
| $V_1$=V, $V_2$=2V, $V_3$=3V | 13 Level |
| $V_1$=V, $V_2$=2V, $V_3$=4V | 15 Level |
| $V_1$=V, $V_2$=3V, $V_3$=4V | 17 Level |
| $V_1$=V, $V_2$=2V, $V_3$=6V | 19 Level |
| $V_1$=V, $V_2$=3V, $V_3$=6V | 21 Level |
| $V_1$=V, $V_2$=3V, $V_3$=7V | 23 Level |
| $V_1$=V, $V_2$=3V, $V_3$=8V | 25 Level |
| $V_1$=V, $V_2$=3V, $V_3$=9V | 27 Level |

## III. METHODOLOGY

As the high frequency-based MCPWM is proposed for the selected topology, the switch logic expression for the generation of each level is need to be designed. According to the MLI theory for the generation of 'r' level (r-1) carriers are needed where (r-1)/2 should be the number of positive and negative carriers respectively. For example, in the case of 7 level design 6 carriers are needed where three are positive and

another three are negative. Fig. 2 shows that how carriers are distributed for 7 level design in the case of PD (all the carriers are in phase) modulation and control strategy. The modulation index (MI) can be changed by changing the amplitude of the modulating signal i.e. the reference sine wave signal.

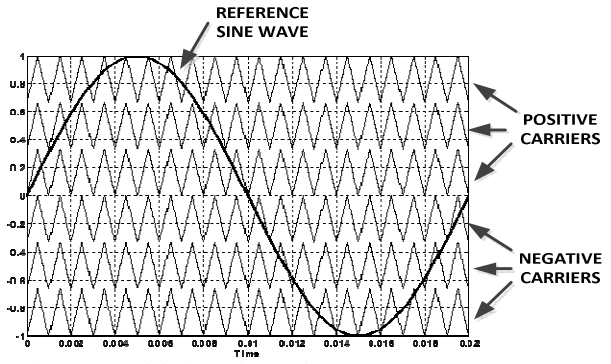


Fig. 2. PD modulation and control strategy.

As with the increase of no. of levels more carriers will be included in the system to generate the higher number of levels, the control technique is getting complicated and requires hard work to design the logical expressions perfectly. For MCPWM control the logical equations are generated according to the switching states with the asymmetrical inputs. Here, a case of 9 level is considered where Table 2 shows the switching states and equations (1) to (4) realize the corresponding logical expressions for 9 level design. Positive carriers are expressed as $CP_1$, $CP_2$, ……,$CP_{(r-1)/2}$, and negative carriers are expressed as $CN_1$, $CN_2$, ……, $CN_{(r-1)/2}$. Symbol '$\oplus$' is used for Boolean XOR operation and '+' is utilized for OR operation.

TABLE II. SWITCHING TECHNIQUES FOR NINE LEVEL DESIGN WITH ASYMMETRICAL INPUT

| **Transistor Activation** | **Corresponding Output Voltage ($V_1$=V, $V_2$=V, $V_3$=2V)** |
|---|---|
| $T_1$, $T_4$, $T_8$, $T_{12}$ | $V_1$ (V) |
| $T_1$, $T_4$, $T_5$, $T_8$, $T_{12}$ | $V_1$+$V_2$ (2V) |
| $T_4$, $T_5$, $T_8$, $T_9$, $T_{12}$ | $V_1$+$V_3$ (3V) |
| $T_1$, $T_4$, $T_5$, $T_8$, $T_9$, $T_{12}$ | $V_1$+ $V_2$+$V_3$ (4V) |
| $T_1$, $T_2$, $T_5$, $T_6$, $T_9$, $T_{10}$ or $T_3$, $T_4$, $T_7$, $T_8$, $T_{11}$, $T_{12}$ | 0V |
| $T_2$, $T_3$, $T_7$, $T_{11}$ | -$V_1$ (-V) |
| $T_2$, $T_3$, $T_6$, $T_7$, $T_{12}$ | -( $V_1$+$V_2$) (-2V) |
| $T_3$, $T_6$, $T_7$, $T_{10}$, $T_{12}$ | -($V_1$+$V_3$) (-3V) |
| $T_2$, $T_3$, $T_6$, $T_7$, $T_{10}$, $T_{12}$ | -($V_1$+ $V_2$+$V_3$) (-4V) |

The logical equations for the 9 level design according to Table II can be written as

$$T_1=(CP_1 \oplus CP_3) + CP_4 \quad (1)$$
$$T_4, T_8, T_{12}=CP_1 \quad (2)$$
$$T_5=CP_2, T_9=CP_3 \quad (3)$$
$$T_2=(CN_1^{/} \oplus CN_3^{/})+CN_4^{/} \quad (4)$$
$$T_3, T_7, T_{11}=CN_1^{/} \quad (5)$$
$$T_6=CN_2^{/}, T_{10}=CN_3^{/} \quad (6)$$

The zero switch logic is $(CP_1 \oplus CN_1)$ which is provided parallel to those transistors that need to be activated during zero voltage levels. From the above expressions it is realized that the transistors are complementary to each other for example if $T_1$ is activated by using positive carriers and logical combinations then a similar combination of negative carriers is required for the activation of the T2 switch, only the difference is for the negative carriers inverted operation is required. In similar fashion $T_3$-$T_4$, $T_5$-$T_6$, $T_7$-$T_8$, $T_9$-$T_{10}$, and $T_{11}$-$T_{12}$, are complementary to each other which is established in equations (1) to (6).

Therefore, the logical expressions for the other levels can be designed by this method but the complexity arises because of an increasing number of levels relating to the same number of switches to be operated. The logical equations for other level generations are shown below one by one from the 11 level to the 27 level. To reduce the size of the paper only positive level generation is realized by using the transistors $T_1$, $T_4$, $T_5$, $T_8$, $T_9$, & $T_{12}$ as the negative levels can be shown with corresponding complementary negative carriers.

11 level inverter logic equations for positive voltage-

$$T_1=(CP_1 \oplus CP_2) + (CP_3 \oplus CP_4) + CP_5 \quad (7)$$
$$T_4, T_8, T_{12}=CP_1 \quad (8)$$
$$T_5=CP_2, T_9=CP_4 \quad (9)$$

13 level inverter logic equations for positive voltage-

$$T_1=(CP_1 \oplus CP_2) + (CP_4 \oplus CP_5) + CP_6 \quad (10)$$
$$T_5=(CP_2 \oplus CP_3) + CP_5 \quad (11)$$
$$T_4, T_8, T_{12}=CP_1 \quad (12)$$
$$T_9=CP_3 \quad (13)$$

15 level inverter logic equations for positive voltage-

$$T_1=(CP_1 \oplus CP_2) + (CP_3 \oplus CP_4) + (CP_5 \oplus CP_6) + CP_7 \quad (14)$$
$$T_5=(CP_2 \oplus CP_4) + CP_6 \quad (15)$$
$$T_4, T_8, T_{12}=CP_1 \quad (16)$$
$$T_9=CP_4 \quad (17)$$

17 level inverter logic equations for positive voltage-

$$T_1=(CP_1 \oplus CP_2) + (CP_5 \oplus CP_6) + CP_8 + (CN_2 \oplus CN_3)+ (CN_6 \oplus CN_7) \quad (18)$$
$$T_4=(CP_1 \oplus CP_2) + (CP_3 \oplus CP_6) + CP_7 + (CN_2 \oplus CN_3)+ (CN_6 \oplus CN_7) \quad (19)$$
$$T_5=(CP_2 \oplus CP_4) + CP_6 \quad (20)$$
$$T_8, T_{12}=CP_1 \quad (21)$$
$$T_9=CP_4 \quad (22)$$

19 level inverter logic equations for positive voltage-

$$T_1=(CP_1 \oplus CP_2) + (CP_3 \oplus CP_4) + (CP_7 \oplus CP_8) + CP_9 + (CN_5 \oplus CN_6) \quad (23)$$
$$T_4=(CP_1 \oplus CP_5) + CP_6+(CN_5 \oplus CN_6) \quad (24)$$
$$T_5=(CP_2 \oplus CP_4) + CP_8+(CN_4 \oplus CN_5) \quad (25)$$
$$T_8=(CP_1 \oplus CP_4) + CP_5+(CN_4 \oplus CN_5) \quad (26)$$
$$T_9=CP_4, T_{12}=CP_1 \quad (27)$$

21 level inverter logic equations for positive voltage-

$$T_1=(CP_1 \oplus CP_2) + (CP_4 \oplus CP_5) + (CP_7 \oplus CP_8) + CP_{10} + (CN_2 \oplus CN_3)+ (CN_5 \oplus CN_6)+ (CN_8 \oplus CN_9) \quad (28)$$

$$T_4=(CP_1 \oplus CP_2) + (CP_3 \oplus CP_5) + (CP_6 \oplus CP_8) + CP_9 + (CN_2 \oplus CN_3)+ (CN_5 \oplus CN_6)+ (CN_8 \oplus CN_9) \quad (29)$$

$$T_5=(CP_2 \oplus CP_5) + CP_8 \quad (30)$$

$$T_8=CP_1, T_9=CP_5, T_{12}=CP_1 \quad (31)$$

23 level inverter logic equations for positive voltage-

$$T_1=(CP_1 \oplus CP_2) + (CP_4 \oplus CP_6) + (CP_8 \oplus CP_9) + CP_{11} + (CN_2 \oplus CN_3)+ (CN_6 \oplus CN_7)+ (CN_9 \oplus CN_{10}) \quad (32)$$

$$T_4=(CP_1 \oplus CP_2) + (CP_3 \oplus CP_6) + (CP_7 \oplus CP_9) + CP_{10} + (CN_2 \oplus CN_3)+ (CN_6 \oplus CN_7)+ (CN_9 \oplus CN_{10}) \quad (33)$$

$$T_5=(CP_2 \oplus CP_5) + CP_9+(CN_5 \oplus CN_6) \quad (34)$$

$$T_8=(CP_1 \oplus CP_5) + CP_6+(CN_5 \oplus CN_6) \quad (35)$$

$$T_9=CP_5, T_{12}=CP_1 \quad (36)$$

25 level inverter logic equations for positive voltage-

$$T_1=(CP_1 \oplus CP_2) + (CP_4 \oplus CP_5) + (CP_6 \oplus CP_7) + (CP_9 \oplus CP_{10}) + CP_{12} + (CN_2 \oplus CN_3)+ (CN_7 \oplus CN_8)+ (CN_{10} \oplus CN_{11}) \quad (37)$$

$$T_4=(CP_1 \oplus CP_2) + (CP_3 \oplus CP_7) + (CP_8 \oplus CP_{10}) + CP_{11} + (CN_2 \oplus CN_3)+ (CN_7 \oplus CN_8)+ (CN_{10} \oplus CN_{11}) \quad (38)$$

$$T_5=(CP_2 \oplus CP_5) + CP_{10}+(CN_5 \oplus CN_7) \quad (39)$$

$$T_8=(CP_1 \oplus CP_5) + CP_7+(CN_5 \oplus CN_7) \quad (40)$$

$$T_9=CP_5, T_{12}=CP_1 \quad (41)$$

27 level inverter logic equations for positive voltage-

$$T_1=(CP_1 \oplus CP_2) + (CP_4 \oplus CP_5) + (CP_7 \oplus CP_8) + (CP_{10} \oplus CP_{11}) + CP_{13} + (CN_2 \oplus CN_3)+ (CN_5 \oplus CN_6)+ (CN_8 \oplus CN_9) + (CN_{11} \oplus CN_{12}) \quad (42)$$

$$T_4=(CP_1 \oplus CP_2) + (CP_3 \oplus CP_5) + (CP_6 \oplus CP_8) + (CP_9 \oplus CP_{11}) + CP_{12} + (CN_2 \oplus CN_3)+ (CN_5 \oplus CN_6)+ (CN_8 \oplus CN_9) + (CN_{11} \oplus CN_{12}) \quad (43)$$

$$T_5=(CP_2 \oplus CP_5) + CP_{11}+(CN_5 \oplus CN_8) \quad (44)$$

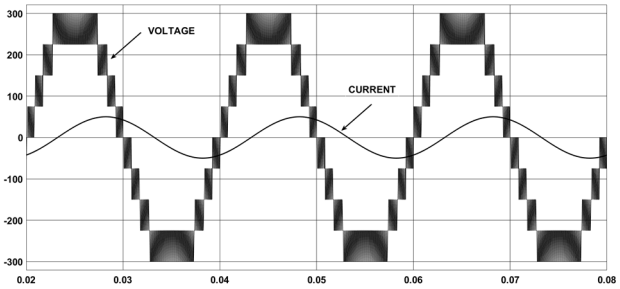
$$T_8=(CP_1 \oplus CP_5) + CP_8+(CN_5 \oplus CN_8) \quad (45)$$

$$T_9=CP_5, T_{12}=CP_1 \quad (46)$$

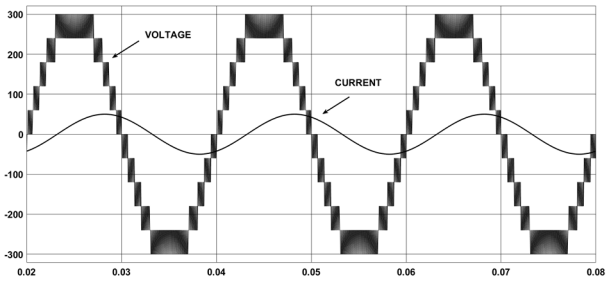
From the above expressions it is realized that with the increase of a number of levels the switching complexity arises more compared to the previous level generations.

## IV. Simulation Results

The proposed inverter is simulated to generate all the levels for asymmetrical switching from 9 level to 27 level with RL load at MATLAB/ SIMULINK environment. The input voltages are selected in such a way that the peak output voltage should vary from 300~330V peak. Fig. 3 shows all the output voltages and currents for the proposed PD-based MCPWM control strategy. From Fig. 3 it is realized that the proposed inverter is capable of generating the required level without increasing the number of switches and component counts further. The FFT spectrum for 27 level design is given in Fig. 4, which shows the lowest THD among all the proposed designs.




(a)

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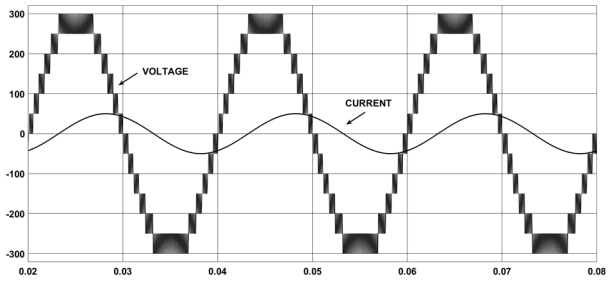
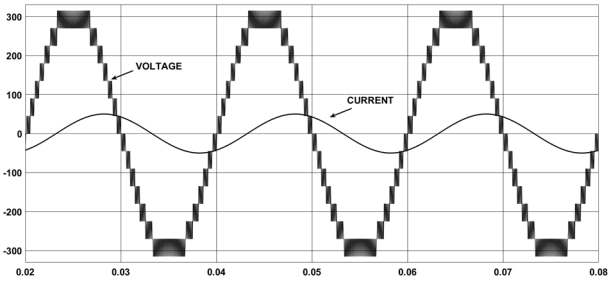
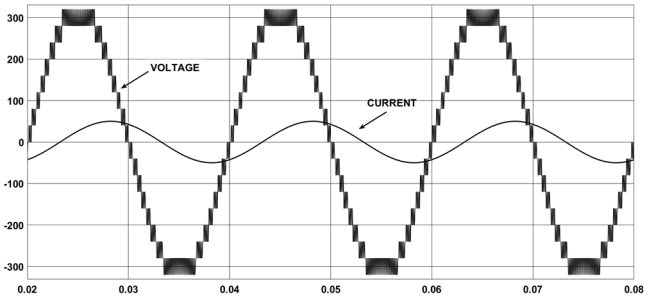


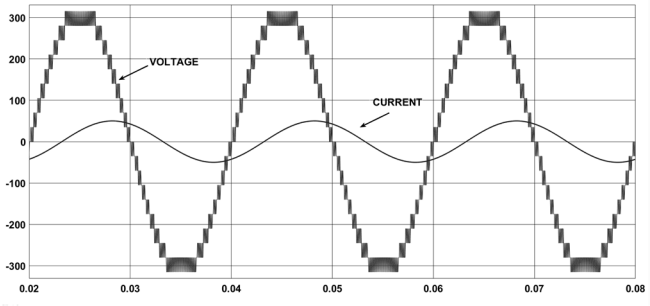

(c)



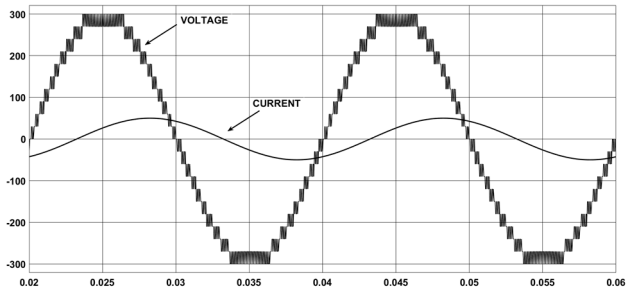

(d)



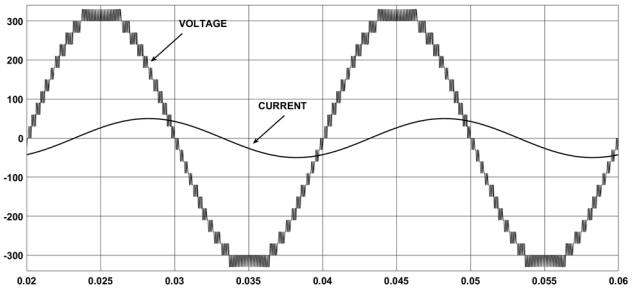

(e)



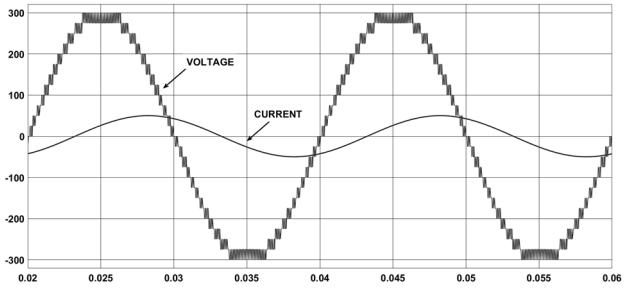

(f)



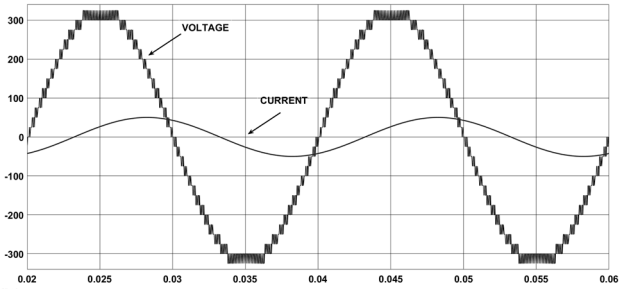

(g)




(h)




(i)




(j)

Fig. 3. Output voltages and currents for all the designed inverters (a) 9 level (b) 11 level (c) 13 level (d) 15 level (e) 17 level (f) 19 level (g) 21 level (h) 23 level (i) 25 level (j) 27 level

The lowest voltage THD value achieved for the proposed inverter is 4.21% which is comparable according to the different codes and standards[4], [5]. It is also clear from the FFT spectrum of Fig. 4 that higher-order harmonics are present in the output which reduces the filter size in the output.

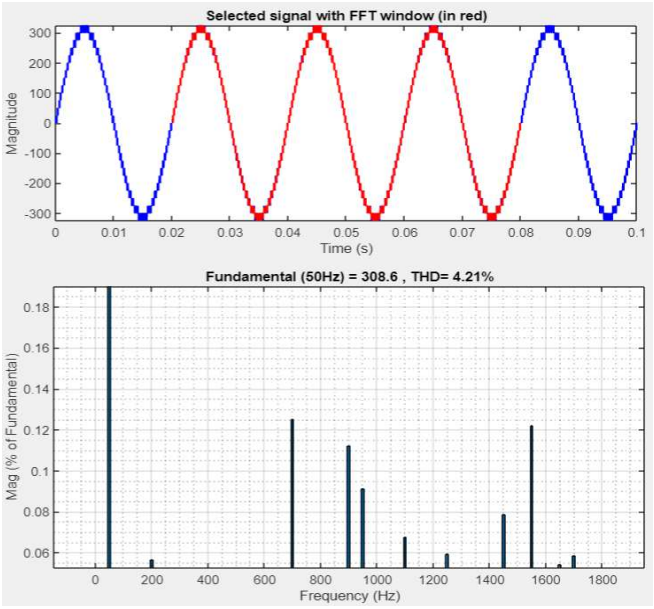



Fig. 4. FFT spectrum for 27 level design.

## V. Conclusion

In this work, authors have tried to focus on high frequency control with asymmetrical switching as the modulation process is highly complex to design for the generation of a higher number of levels. The selected CHB topology is suitable for the generation of a higher number of levels as it has negative switching redundancy. The control logic which are developed is feasible and can be applied for a higher number of levels generation by using the more switch CHB topology. The proposed inverter with MCPWM control can be particularly suitable as a standalone or grid-tied solar inverter.

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